

**TITLE : DV430QUB-P10****Product Specification****Fuzhou BOE Optoelectronics Technology Co., Ltd**SPEC. NUMBER  
S8-64-8D-049PRODUCT GROUP  
TFT-LCD

Rev. O

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1 OF 36

**REVISION HISTORY** Preliminary specification Final specification

Revision No.	Page	Description of changes	Date	Prepared
P0	-	Initial Release	2020.04.03	Jiang Shunwang
P1	25	Frame Rate Update	2020.04.07	Jiang Shunwang

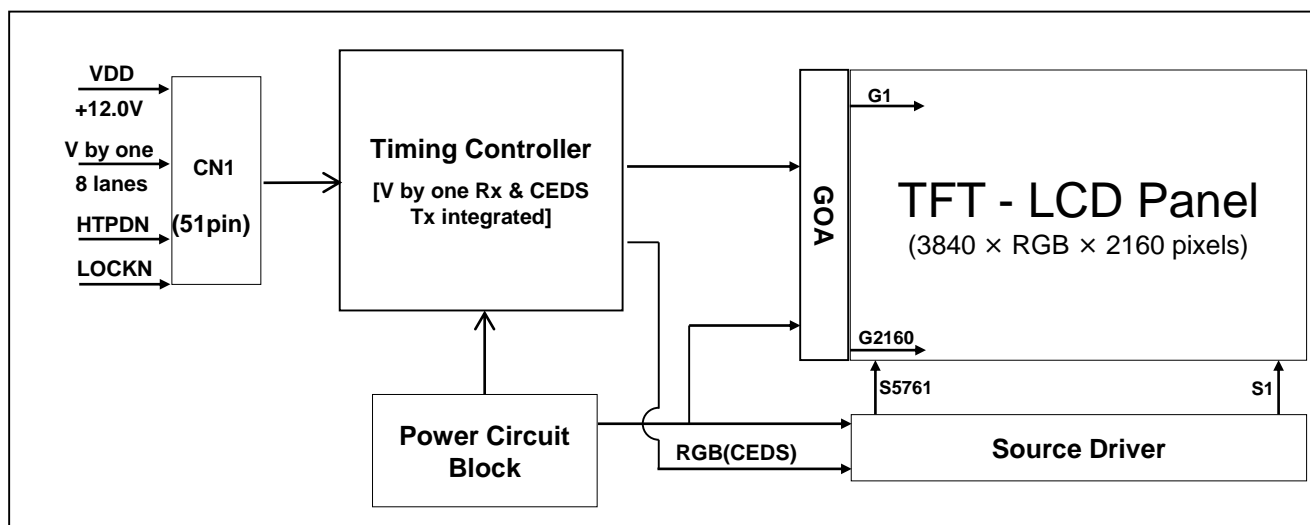
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## 1.0 GENERAL DESCRIPTION

### 1.1 Introduction

DV430QUB-P10 is a color active matrix TFT LCD open cell using amorphous silicon TFT's (Thin Film Transistors) as an active switching device. This module has a 43 inch diagonally measured active area with UHD resolutions (3840 horizontal by 2160 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in island and this module can display 1.07G colors. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.



### 1.2 Features

- V by one interface with 8 lanes
- High-speed response
- Low color shift image quality
- 8-bit + FRC color depth, display 1.07G colors
- High luminance and contrast ratio, low reflection and wide viewing angle
- DE (Data Enable) only mode
- ADS technology is applied for high display quality
- RoHS compliant
- Support 7\*24hr

**1.0 GENERAL DESCRIPTION****1.3 Application**

- Home Alone Multimedia TFT-LCD TV
- Display Terminals for Control System
- Ultra High Definition TV(UHD TV)
- AV application Products

**1.4 General Specification**

&lt; Table 1. General Specifications &gt;

Parameter	Specification	Unit	Remark
Active area	941.184(H) × 529.416 (V)	mm	
Number of pixels	3840*(RGB)*2160	pixels	
Pixel pitch	81.7(H) × 245.1 (V)	μm	
Pixel arrangement	Pixels RGB Island		
Display colors	1.07G (8bits + FRC )	colors	
Display mode	Transmission mode, Normally Black		
Possible Display Type	Landscape and Portrait Enabled	-	
Open Cell Transmittance	4.1	%	At center point with BOE BLU
Weight	1.58	Kg	
Power Consumption	9.6(Typ.)	Watt	With TCON Board
Surface Treatment	Haze 1%, 3H, Semi-glare or Anti-glare treatment (Front Polarizer) Clear (Bottom Polarizer)		

### 2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

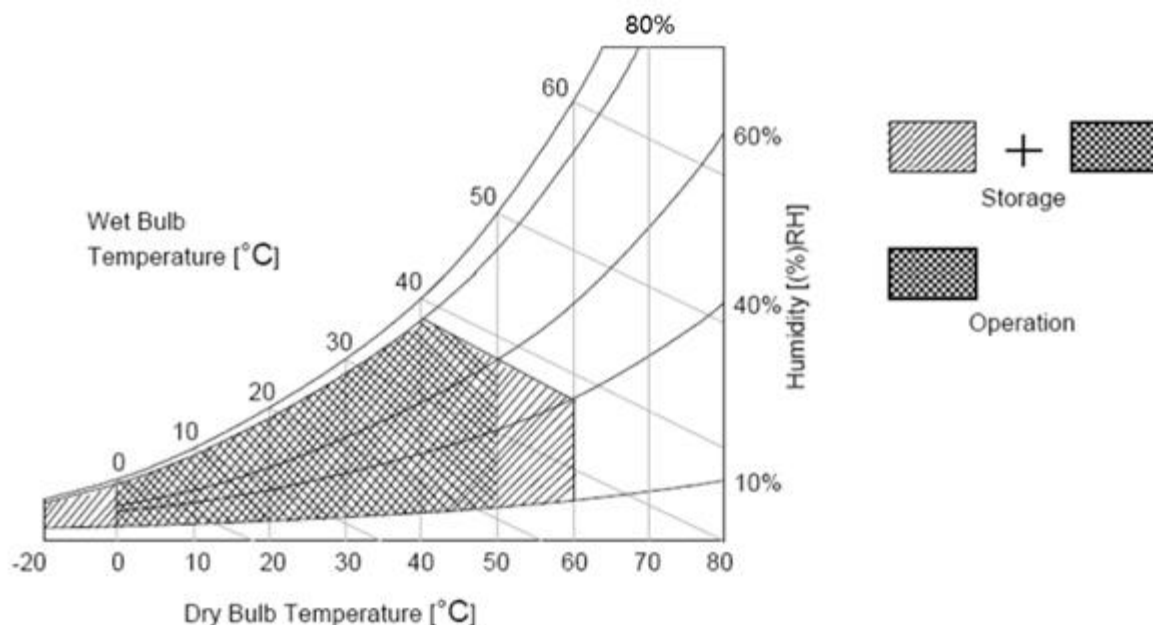
< Table 2. Open Cell Absolute Maximum Ratings >

[VSS=GND=0V]

Parameter	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD	VSS-0.3	13.2	V	Ta = 25 °C
Operating Temperature	T <sub>OP</sub>	0	+50	°C	Note 1
Storage Temperature	T <sub>SUR</sub>	-20	+60	°C	
	T <sub>ST</sub>	-20	+60	°C	
Operating Ambient Humidity	Hop	10	80	%RH	
Storage Humidity	Hst	10	80	%RH	

Note 1 : Temperature and relative humidity range are shown in the figure below.

Note 2 : Wet bulb temperature should be 39 °C max. and no condensation of water.



### 3.0 ELECTRICAL SPECIFICATIONS

#### 3.1 TFT LCD Open Cell

< Table 3. Open Cell Electrical Specifications >

[Ta =25±2 °C]

Parameter	Symbol	Values			Unit	Remark	
		Min	Typ	Max			
Power Supply Input Voltage	VDD	10.8	12	13.2	Vdc		
Power Supply Ripple Voltage	VRP	-	-	600	mV		
Power Supply Current	IDD	-	0.8	2.3	A	Note 1	
Power Consumption	PDD		9.6	27	Watt		
Rush current	IRUSH	-	-	10	A	Note 2	
V by One Interface	Differential Input High Threshold Voltage	VLVTH	-	-	+50	mV	
	Differential Input Low Threshold Voltage	VLVTL	-50	-	-	mV	
	Common Input Voltage	VLVC	-	-	-	V	
	Terminating Resistor	Rt	90	100	110	ohm	
CMOS Interface	Input High Threshold Voltage	VIH	2.0	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.8	V	

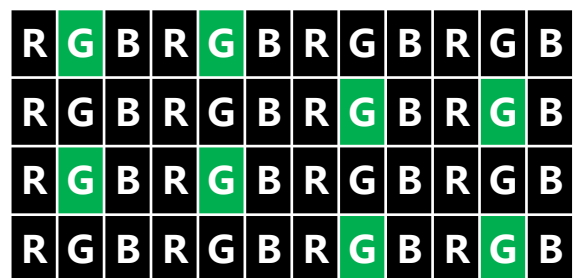
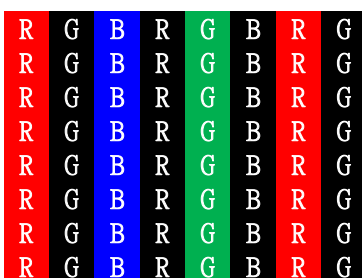
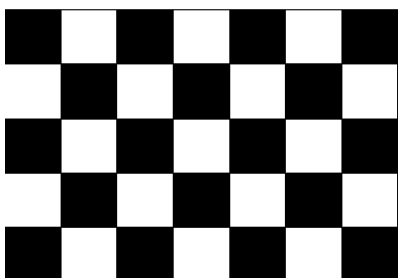
Note 1 : The supply voltage is measured and specified at the interface connector of LCM.

The current draw and power consumption specified is for VDD=12.0V.

a) Typ: Mosaic 7X5(L0/L255)

b) Max : Vertical Sub Line(L255)

c) Flicker Test Pattern



Note 2 : The duration of rush current is about 2ms and rising time of Power Input is 1ms(min).

### 3.0 ELECTRICAL SPECIFICATIONS

#### 3.2 IC Characteristics

< Table 4. TCON Characteristics >

Parameter	Symbol	Values			Unit	Remark
		Min	Typ	Max		
TCON Surface Temperature	$T_{TS}$	-	-	110	°C	Note

Note 1 : Any point on the TCON surface must be less than 110 °C under any conditions.

Note 2 : This test condition is based on BOE module.

< Table 5. Driver Characteristics >

Parameter	Symbol	Values			Unit	Remark
		Min	Typ	Max		
Driver Surface Temperature	$T_{DS}$	-	-	125	°C	Note

Note 3 : Any point on the driver surface must be less than 125 °C under any conditions.

Note 4: This test condition is based on BOE module.

< Table 6. PMIC Characteristics >

Parameter	Symbol	Values			Unit	Remark
		Min	Typ	Max		
PMIC Surface Temperature	$T_{PS}$	-	-	100	°C	Note

Note 5 : Any point on the PMIC surface must be less than 100 °C under any conditions.

Note 6: This test condition is based on BOE module.



### 3.0 ELECTRICAL SPECIFICATIONS

#### 3.3 VCOM tuning SOP

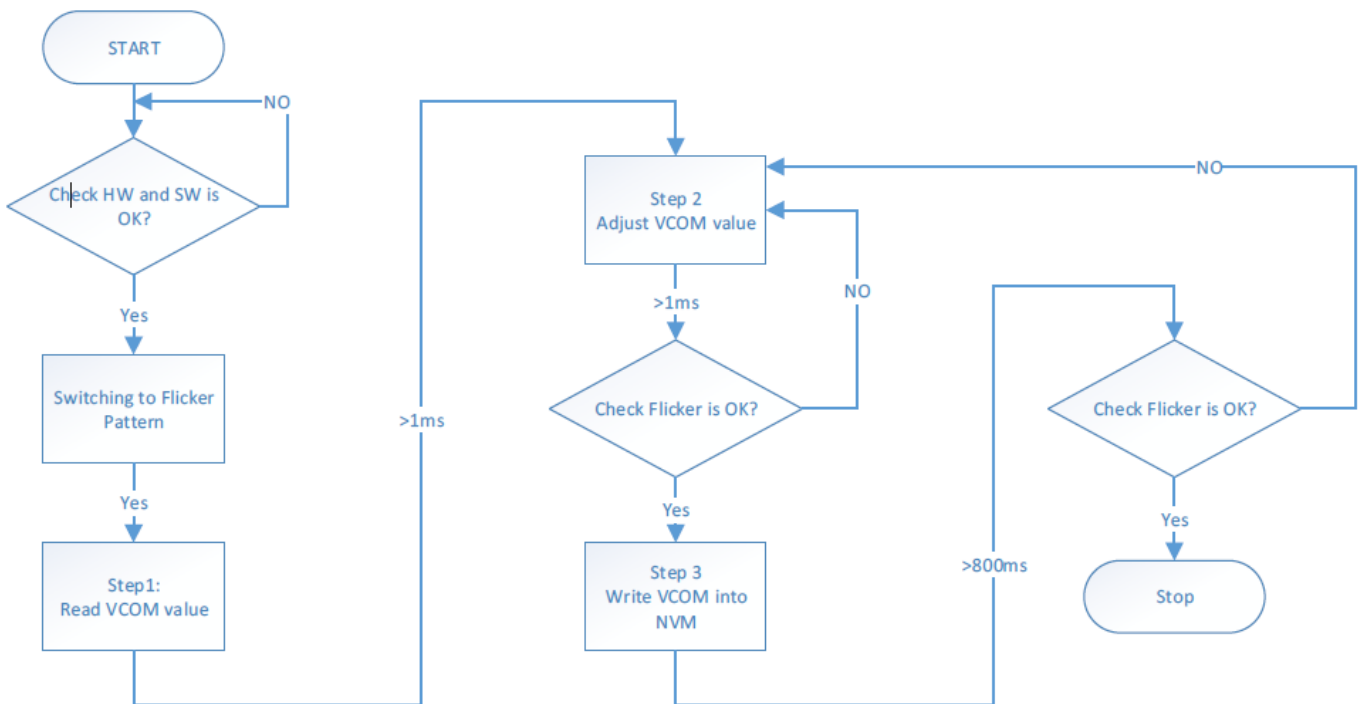
1. Check Hardware A0 pin setting and use corresponding I2C VCOM commend.

A0			
Hardware Setting		Software Setting	
		Read	Write
A0=L Level		0b01000001 (0x41)	0b01000000 (0x40)
A0= H Level		0b01000011 (0x43)	0b01000010 (0x42)

Note1: 0b: binary, 0x: hex

Note2: taking A0=0 for below example.

2. Flow chart



### 3.0 ELECTRICAL SPECIFICATIONS

Note 3:

Data @ reg25h is from 0x00 (0b00000000) to 0x03 (0b00000011)

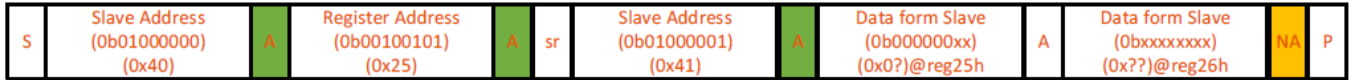
Data @ reg26h is from 0x00 (0b00000000) to 0xFF (0b11111111)

[reg25h reg26h] = 0x0000 to 0x03FF

MSB of VCOM is b2@reg25h, and LSB is b0@reg26h

Default			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
25h	[7:0]	02h	-	-	-	-	-	-	VC[9]	VC[8]
26h	[7:0]	00h	VC[7]	VC[6]	VC[5]	VC[4]	VC[3]	VC[2]	VC[1]	VC[0]

#### 3. Step1: Read NVM VCOM Value



#### 4. Step 2 Adjust VCOM Value



#### 5. Step 3 Write VCOM Value into NVM



Note 4:



### 4.0 INTERFACE CONNECTION

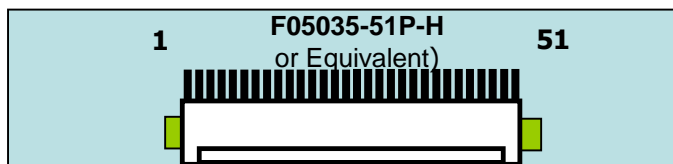
4.1 V by One CN (51Pin) Connector : F05035-51P-H or PM.FPC.LVS0505101 or Equivalent.

< Table 7. Open Cell Input Connector Pin Configuration >

Pin No	Symbol	Description	Pin No	Symbol	Description
1	VDD	Power Supply +12.0V	27	GND	Ground
2	VDD	Power Supply +12.0V	28	Rx0n	V-by-One HS Data Lane 0
3	VDD	Power Supply +12.0V	29	Rx0p	V-by-One HS Data Lane 0
4	VDD	Power Supply +12.0V	30	GND	Ground
5	VDD	Power Supply +12.0V	31	Rx1n	V-by-One HS Data Lane 1
6	VDD	Power Supply +12.0V	32	Rx1p	V-by-One HS Data Lane 1
7	VDD	Power Supply +12.0V	33	GND	Ground
8	VDD	Power Supply +12.0V	34	Rx2n	V-by-One HS Data Lane 2
9	NC	No Connection	35	Rx2p	V-by-One HS Data Lane 2
10	GND	Ground	36	GND	Ground
11	GND	Ground	37	Rx3n	V-by-One HS Data Lane 3
12	GND	Ground	38	Rx3p	V-by-One HS Data Lane 3
13	GND	Ground	39	GND	Ground
14	GND	Ground	40	Rx4n	V-by-One HS Data Lane 4
15	NC	No Connection	41	Rx4p	V-by-One HS Data Lane 4
16	NC	No Connection	42	GND	Ground
17	NC	No Connection	43	Rx5n	V-by-One HS Data Lane 5
18	SDA	SDA	44	Rx5p	V-by-One HS Data Lane 5
19	SCL	SCL	45	GND	Ground
20	NC	No Connection	46	Rx6n	V-by-One HS Data Lane 6
21	NC	No Connection	47	Rx6p	V-by-One HS Data Lane 6
22	SEL_SECTION	Low or NC: 1 section(default) High: 2 section	48	GND	Ground
23	NC	No Connection	49	Rx7n	V-by-One HS Data Lane 7
24	GND	Ground	50	Rx7p	V-by-One HS Data Lane 7
25	HTPDN	Hot plug detect	51	GND	Ground
26	LOCKN	Lock detect			

Note : NC(Not Connected) : These pins are only used for BOE internal operations.

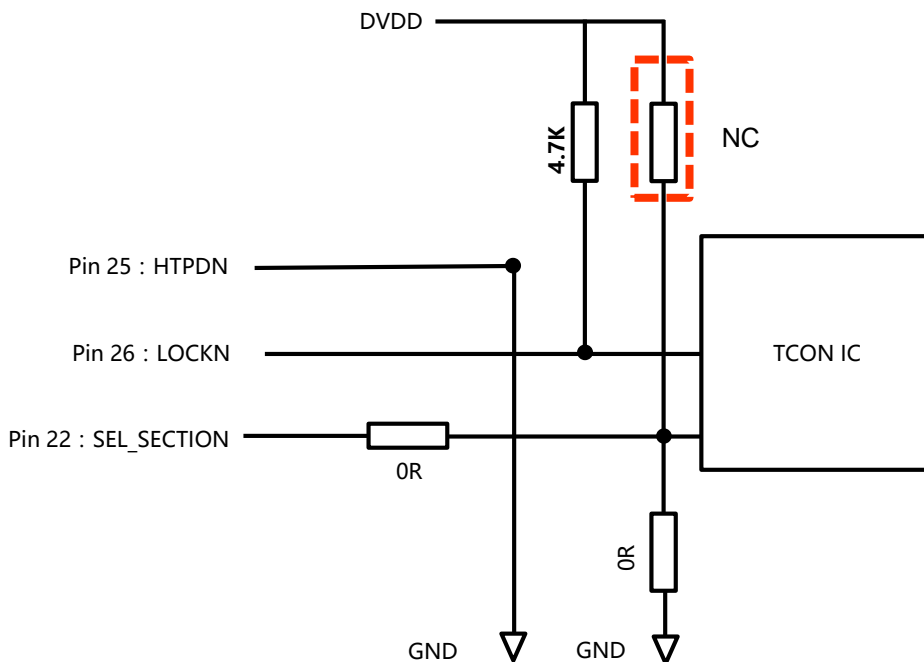
#### Rear view of LCM



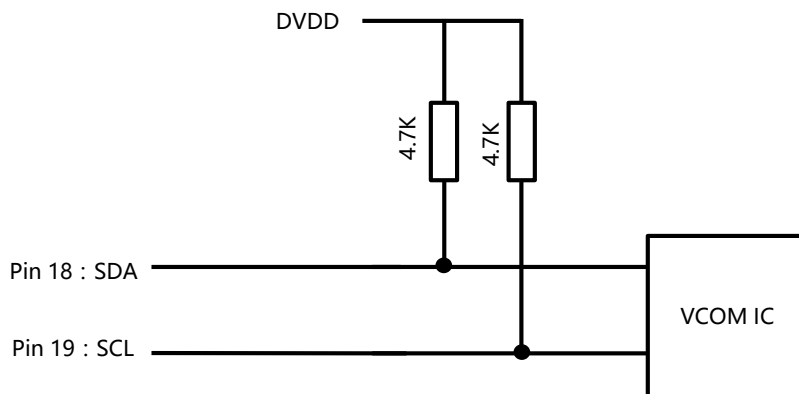
#### BIST Pattern

PT1: Black (2 sec)	PT2: White (2 sec)	PT3: Red (2 sec)	PT4: Green (2 sec)	PT5: Blue (2 sec)

- Notes :
1. NC (Not Connected) : This pins are only used for BOE internal operations.
  - 2.BIST : This pin is used for selecting display pattern mode when input DE or input CLOCK quits toggling.
  3. Circuit Block Diagram of HTPDN/LOCKN/SEL\_SECTION.



4. Circuit Block Diagram Pin of SDA/SCL/WP.



### 4.0 INTERFACE CONNECTION

#### 4.2 V by one Misc. Setting for 1 Section.

- a) System side has to put pull high resistor on LOCKN & HTPDN pins.
- b) V by one data mapping as follows.

< Table 8. V by one setting & data mapping table >

1 Section								
Hactive = 3840								
	Port0		Port1		Port2		Port3	
	Lane0	Lane1	Lane2	Lane3	Lane4	Lane5	Lane6	Lane7
V Blanking	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS
	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP
	...	...	...	...	...	...	...	...
	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP
	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR
Line 1	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8
	Pixel 9	Pixel 10	Pixel 11	Pixel 12	Pixel 13	Pixel 14	Pixel 15	Pixel 16
	...	...	...	...	...	...	...	...
	...	...	...	...	...	...	...	...
	Pixel 3833	Pixel 3834	Pixel 3835	Pixel 3836	Pixel 3837	Pixel 3838	Pixel 3839	Pixel 3840
H Blanking	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS
	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP
	...	...	...	...	...	...	...	...
	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP
	FSBE	FSBE	FSBE	FSBE	FSBE	FSBE	FSBE	FSBE
Line 2	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8
	Pixel 9	Pixel 10	Pixel 11	Pixel 12	Pixel 13	Pixel 14	Pixel 15	Pixel 16
	...	...	...	...	...	...	...	...
	...	...	...	...	...	...	...	...
	Pixel 3833	Pixel 3834	Pixel 3835	Pixel 3836	Pixel 3837	Pixel 3838	Pixel 3839	Pixel 3840

### 4.0 INTERFACE CONNECTION

#### 4.3 V by one Misc. Setting for 2 Section.

- a) System side has to put pull high resistor on LOCKN & HTPDN pins.
- b) V by one data mapping as follows.

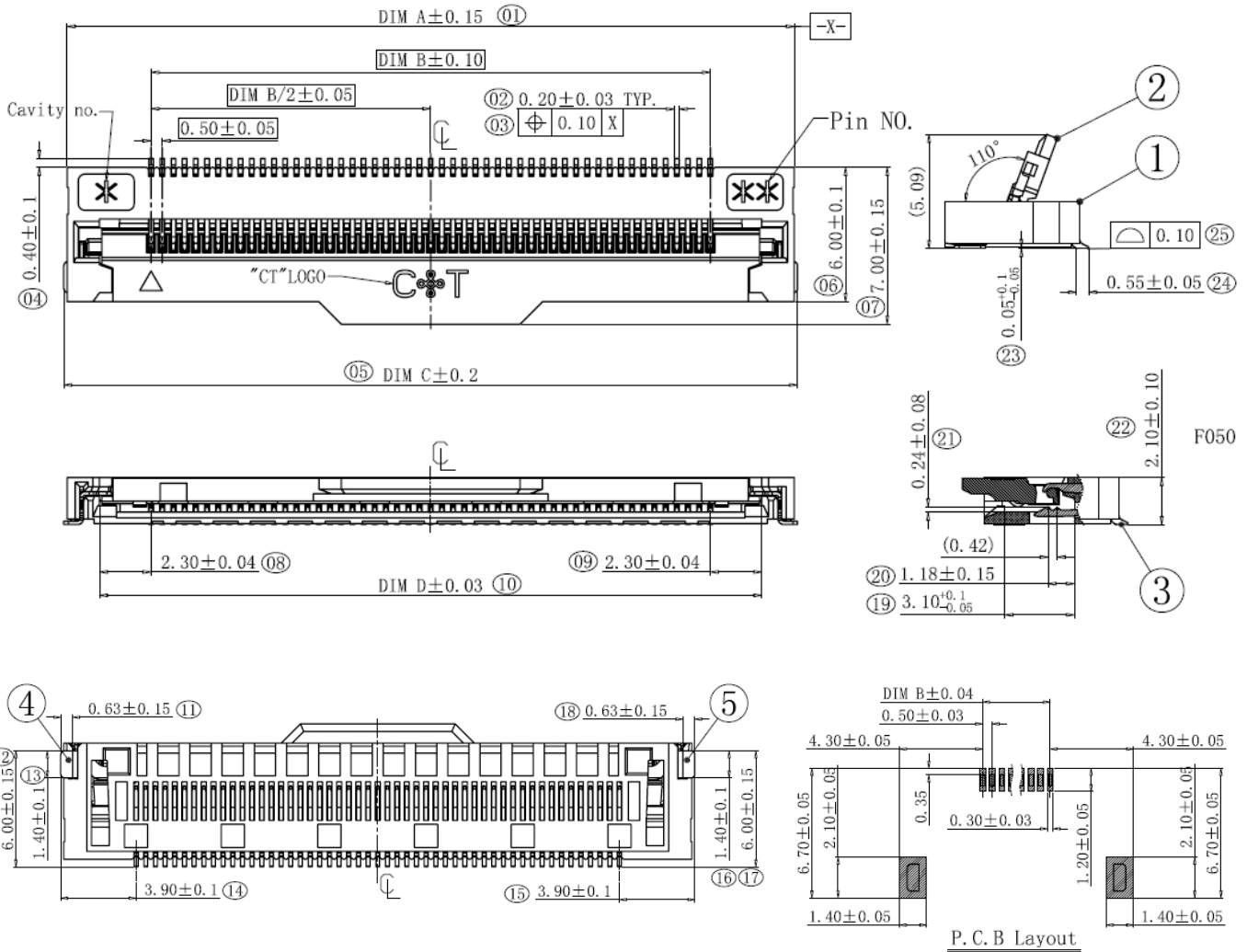
< Table 9. V by one setting & data mapping table >

2 Section								
Hactive = 3840								
	Port0		Port1		Port2		Port3	
	Lane0	Lane1	Lane2	Lane3	Lane4	Lane5	Lane6	Lane7
V Blanking	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS
	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP
	...	...	...	...	...	...	...	...
	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP
	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR
Line 1	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 1921	Pixel 1922	Pixel 1923	Pixel 1924
	Pixel 5	Pixel 6	Pixel 7	Pixel 8	Pixel 1925	Pixel 1926	Pixel 1927	Pixel 1928
	...	...	...	...	...	...	...	...
	...	...	...	...	...	...	...	...
	Pixel 1917	Pixel 1918	Pixel 1919	Pixel 1920	Pixel 3837	Pixel 3838	Pixel 3839	Pixel 3840
H Blanking	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS
	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP
	...	...	...	...	...	...	...	...
	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP	FSBP
	FSBE	FSBE	FSBE	FSBE	FSBE	FSBE	FSBE	FSBE
Line 2	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 1921	Pixel 1922	Pixel 1923	Pixel 1924
	Pixel 5	Pixel 6	Pixel 7	Pixel 8	Pixel 1925	Pixel 1926	Pixel 1927	Pixel 1928
	...	...	...	...	...	...	...	...
	...	...	...	...	...	...	...	...
	Pixel 1917	Pixel 1918	Pixel 1919	Pixel 1920	Pixel 3837	Pixel 3838	Pixel 3839	Pixel 3840

## 4.0 INTERFACE CONNECTION

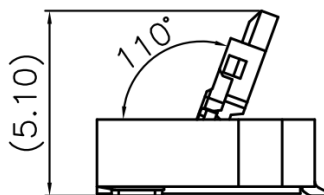
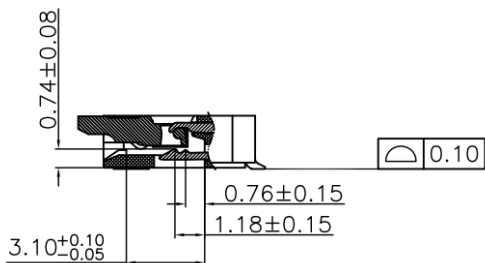
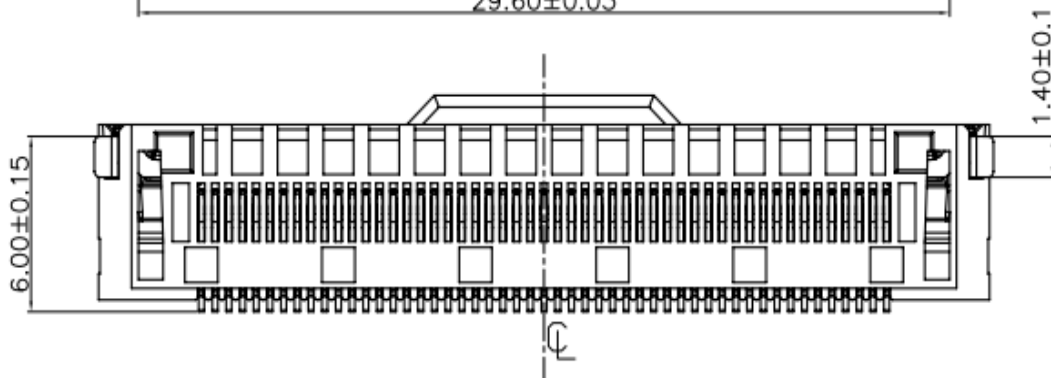
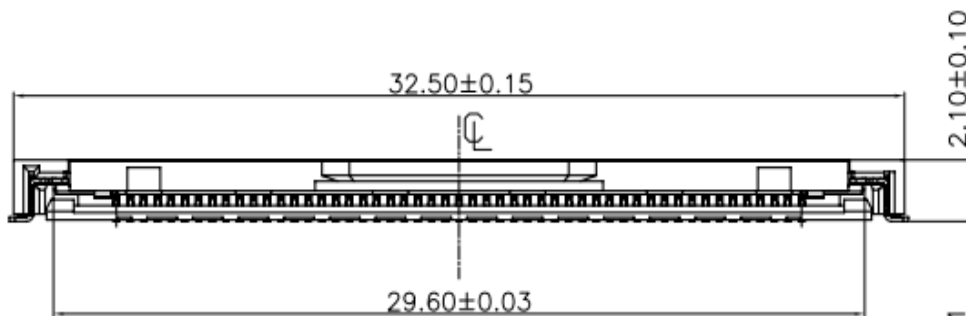
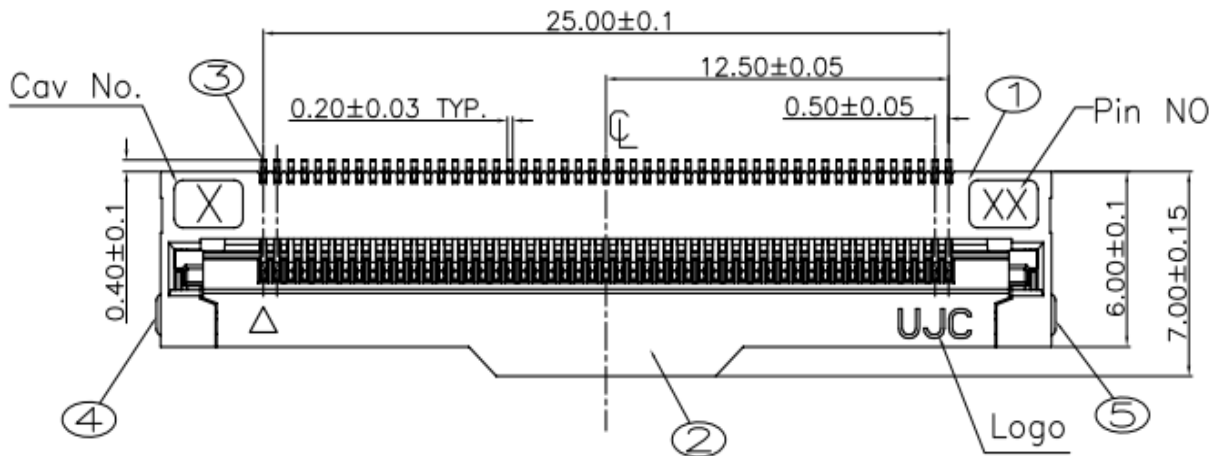
### 4.4 TCON Board Input CNT & FFC Drawing

#### -51pin Connector Drawing-F05035-51P-H



PIN NO.	DIM A	DIM B	DIM C	DIM D
30	22.00	14.50	22.30	19.10
41	27.50	20.00	27.80	24.60
51	32.50	25.00	32.80	29.60

### -51pin Connector Drawing-PM.FPC.LVS0505101

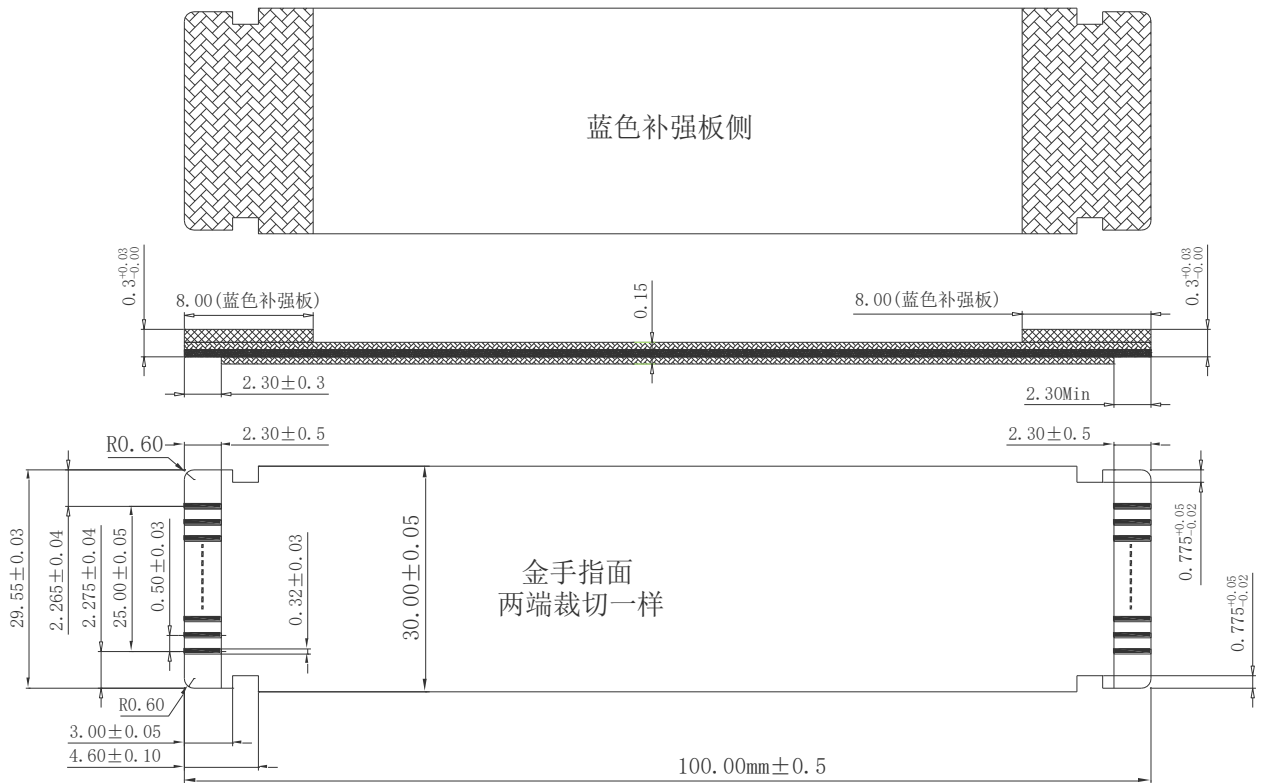




## 4.0 INTERFACE CONNECTION

### 4.4 TCON Board Input CNT & FFC Drawing

#### -VBO FFC Drawing

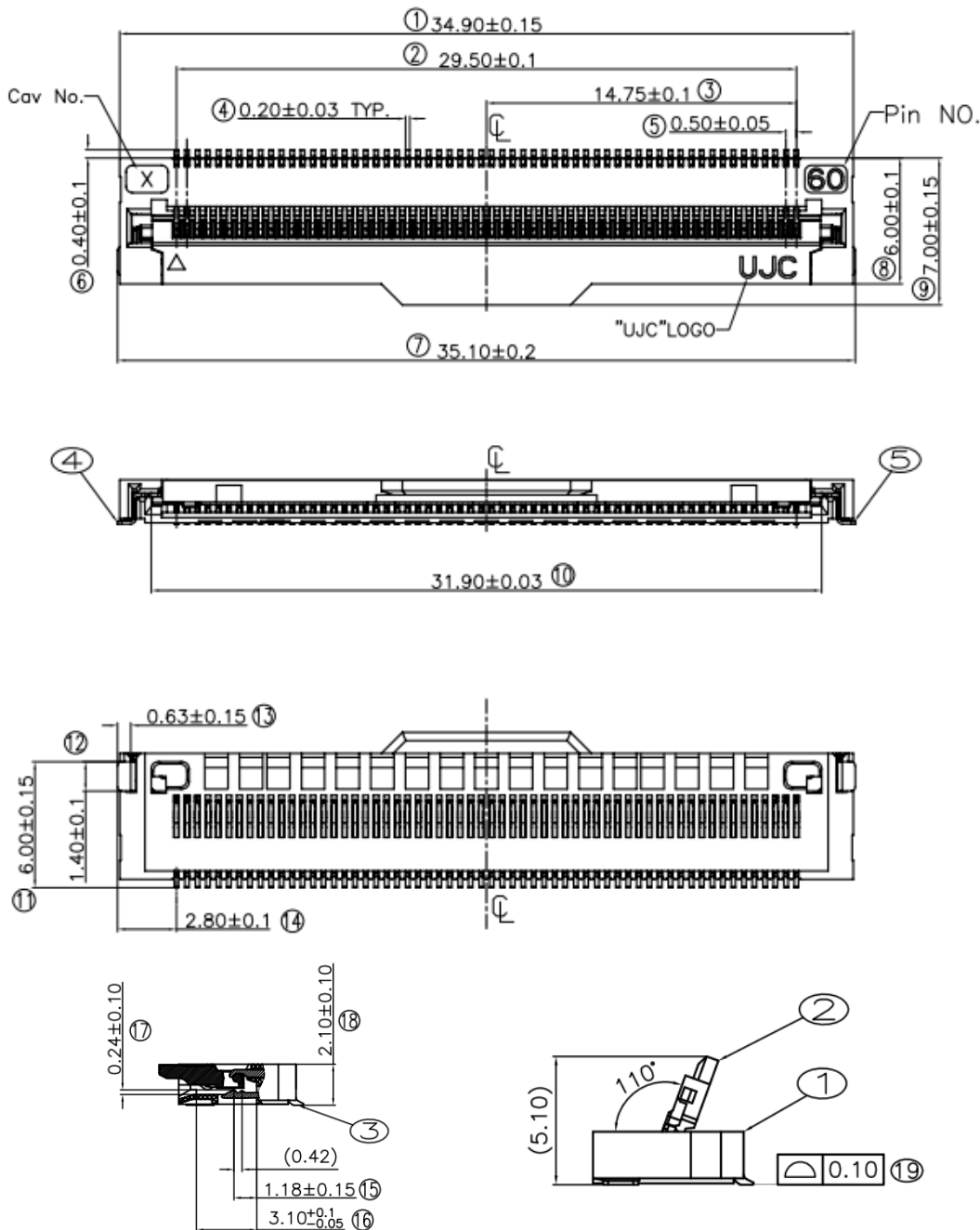


Note: It is BOE FFC drawing. Please refer to only one side for T-con Board.

### 4.0 INTERFACE CONNECTION

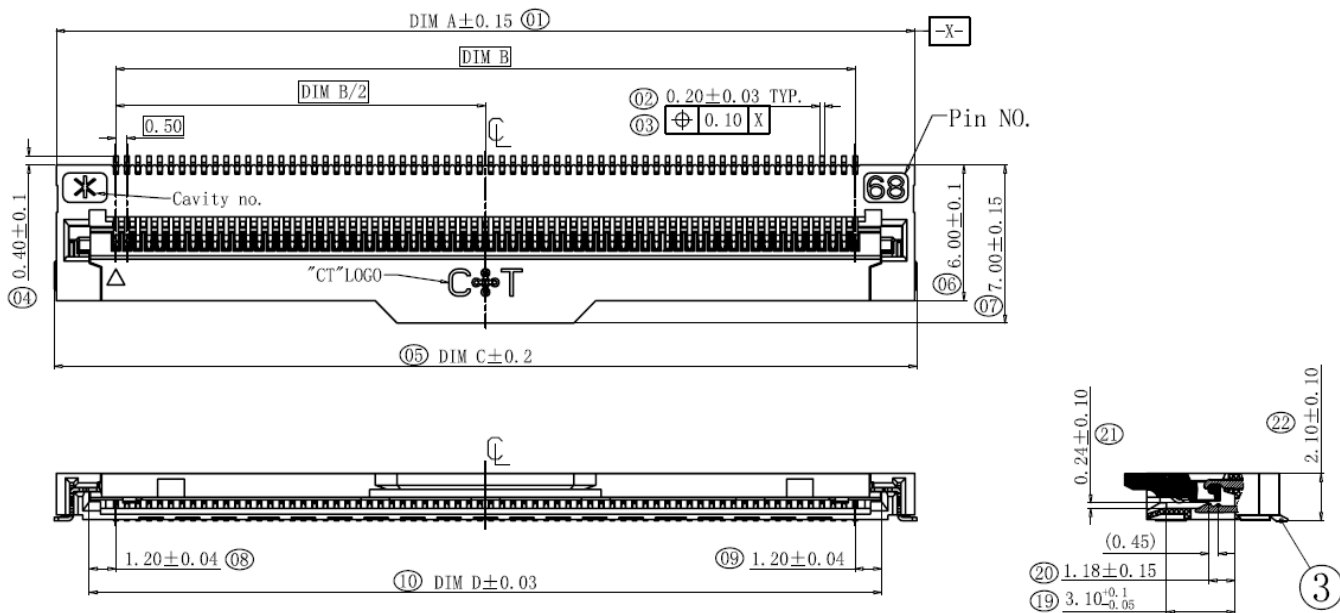
#### 4.5 TCON Board Output CNT & FFC Drawing

##### -60pin Connector Drawing-PM.FPC.LVS0506001



Note: TCON Board output CNT = XPCBA Input CNT.

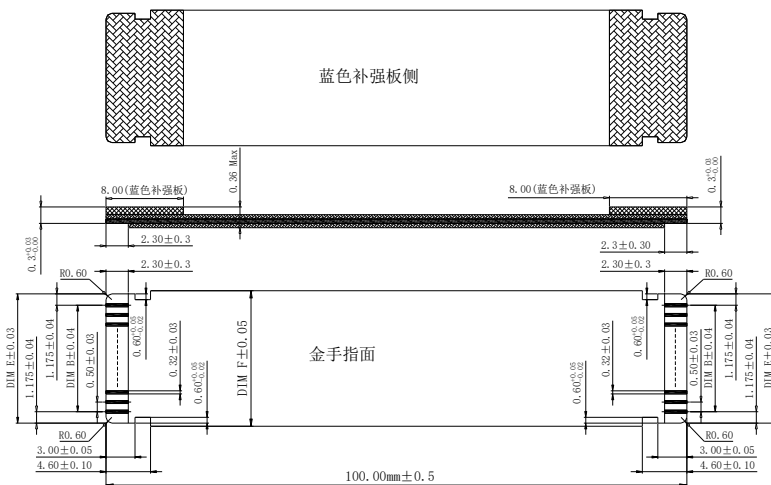
### -60pin Connector Drawing-F05039-60P-H



PIN NO.	DIM A	DIM B	DIM C	DIM D
60	34.90	29.50	35.10	31.90

Note: TCON Board output CNT = XPCBA Input CNT.

### -FFC Drawing



PIN NO.	DIM B	DIM E	DIM F	DIM G	DIM H	排线料号
60	29.50	31.85	32.50	30.50	32.20	F05039-60P-D100

Notes: This FFC drawing is supplied by the connector vendor.

### 5.0 SIGNAL TIMING WAVEFORMS OF INTERFACE SIGNAL

#### 5.1 Input data specification

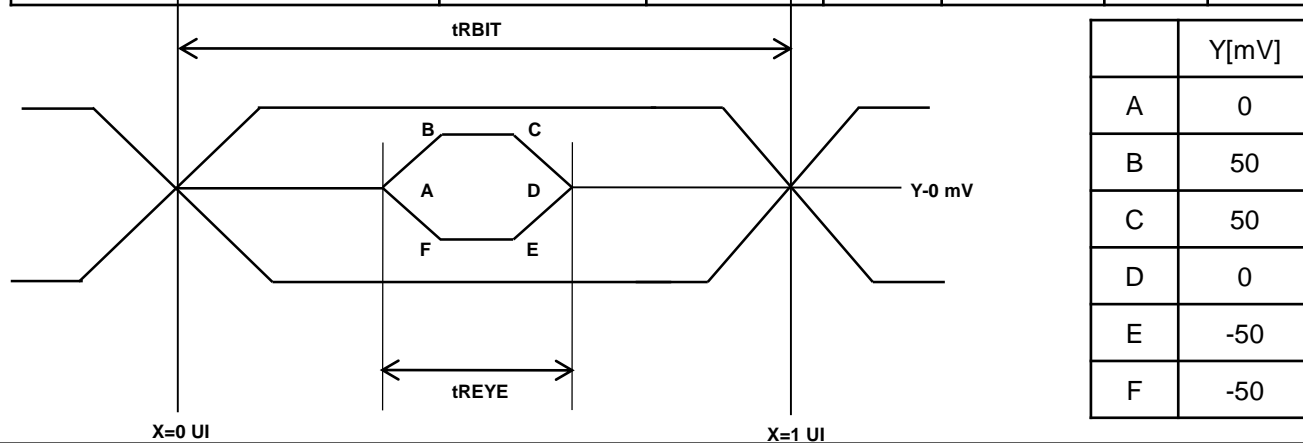
<Table 10. Vx1 Byte length and Color mapping>

Byte	Packer input	Color data mapping
		30 bpp RGB
0	Bit-0	R2
	Bit-1	R3
	Bit-2	R4
	Bit-3	R5
	Bit-4	R6
	Bit-5	R7
	Bit-6	R8
	Bit-7	R9
1	Bit-8	G2
	Bit-9	G3
	Bit-10	G4
	Bit-11	G5
	Bit-12	G6
	Bit-13	G7
	Bit-14	G8
	Bit-15	G9
2	Bit-16	B2
	Bit-17	B3
	Bit-18	B4
	Bit-19	B5
	Bit-20	B6
	Bit-21	B7
	Bit-22	B8
	Bit-23	B9
3	Bit-24	-
	Bit-25	-
	Bit-26	B0
	Bit-27	B1
	Bit-28	G0
	Bit-29	G1
	Bit-30	R0
	Bit-31	R1

### 5.2 Vx1 Input Signal Timing

< Table 11. Signal Timing Waveforms Table >

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Unit Interval(VBO Operation Bit Rate)	tRBIT	3-byte	380	tTCIP/30	1667	PS
		4-byte	285	tTCIP/40	1250	PS
		5-byte	266	tTCIP/50	1000	PS
Eye Width at Package Pin	tREYE	-	-	0.5	-	UI
Eye Width Position A at Package Pin	tA	-	-	0.25	-	UI
Eye Width Position B at Package Pin	tB	-	-	0.3	-	UI
Eye Width Position Cat Package Pin	tC	-	-	0.7	-	UI
Eye Width Position D at Package Pin	tD	-	-	0.75	-	UI
Eye Width Position E at Package Pin	tE	-	-	0.7	-	UI
Eye Width Position F at Package Pin	tF	-	-	0.3	-	UI
Intra – pair Skew	TTOSK_intra	-	-0.3	-	0.3	UI
Inter – pair Skew	TTOSK_inter	-	-5	-	5	UI
SSCG	-	30KHz modulation	-0.5	-	0.5	%



### 6.0 SIGNAL TIMING SPECIFICATION

#### 6.1 Timing Parameters(DE only mode)

< Table 12. Timing Table >

Item		Symbols	Min	Typ	Max	Unit
Frequency		1/Tc	69	74.25	75	MHz
Vertical	Frame Rate	F	57	60	62	Hz
	Total	T <sub>V</sub>	2200	2250	2330	T <sub>H</sub>
	Display	T <sub>VD</sub>	2160			T <sub>H</sub>
	Blank	T <sub>VB</sub>	40	90	170	T <sub>H</sub>
Horizontal	Total	T <sub>H</sub>	530	550	570	T <sub>CLK</sub>
	Display	T <sub>HD</sub>	-	480	-	T <sub>CLK</sub>
	Blank	T <sub>HB</sub>	50	70	90	T <sub>CLK</sub>

Item		Symbols	Min	Typ	Max	Unit
Frequency		1/Tc	69	74.25	75	MHz
Vertical	Frame Rate	F	47	50	51	Hz
	Total	T <sub>V</sub>	2200	2700	2715	T <sub>H</sub>
	Display	T <sub>VD</sub>	2160			T <sub>H</sub>
	Blank	T <sub>VB</sub>	40	540	555	T <sub>H</sub>
Horizontal	Total	T <sub>H</sub>	530	550	570	T <sub>CLK</sub>
	Display	T <sub>HD</sub>	-	480	-	T <sub>CLK</sub>
	Blank	T <sub>HB</sub>	50	70	90	T <sub>CLK</sub>

Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

### 6.0 SIGNAL TIMING SPECIFICATION

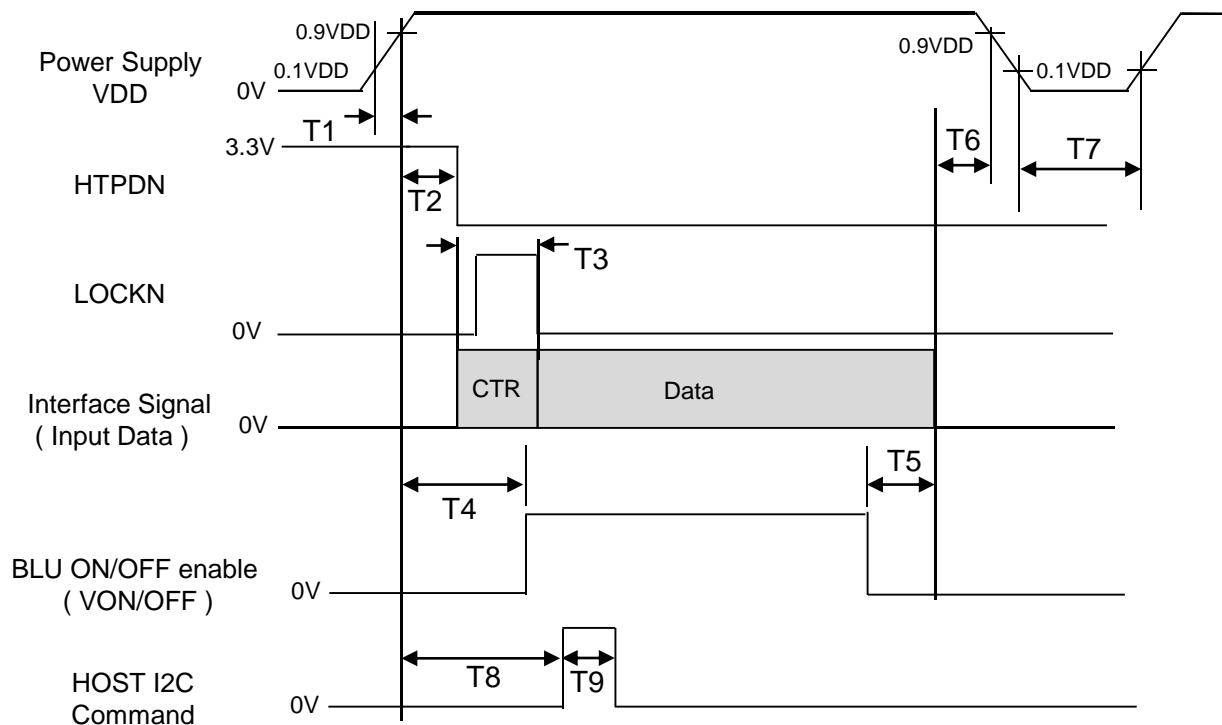
#### 6.3 Input Signals, Basic Display Colors and Gray Scale of Colors

< Table 13. Input Signal and Display Color Table >

Color		Input Color Data																											
		MSB RED LSB										MSB GREEN LSB										MSB BLUE LSB							
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	RED(001)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	----																												
	RED(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	RED(1023)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
G	Green (000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green (000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	
	----																												
	Green (1022)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	
	Green (1023)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
B	Blue(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	----																												
	Blue(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

## 6.0 SIGNAL TIMING SPECIFICATION

### 6.4 Power Sequence



< Table 7. Sequence Table >

Parameter	Values			Units
	Min	Typ	Max	
T1	0.5	-	10	ms
T2	0	-	-	ms
T3	-	-	500	ms
T4	T2+T3	-	-	-
T5	100	-	-	ms
T6	0	-	-	ms
T7	1	-	-	s
T8	1	-	-	s
T9	Depends on I2C command			ms

- Notes:
1. Even though T1 is over the specified value, there is no problem if I2T spec of fuse is satisfied.
  2. Back Light must be turn on after power for logic and interface signal are valid.
  3. BLU enable must after input data.
  4. HOST I2C operate after BLU enable.



## 7.0 OPTICAL SPECIFICATION

The test of optical specifications shall be measured in a dark room (ambient luminance $\leq$ 1 lux and temperature $=25\pm 2^{\circ}\text{C}$ ) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 180cm from the LCD surface at a viewing angle of  $\theta$  and  $\Phi$  equal to  $0^{\circ}$ . We refer to  $\theta_{\phi=0}$  ( $=\theta_3$ ) as the 3 o'clock direction (the "right"),  $\theta_{\phi=90}$  ( $=\theta_{12}$ ) as the 12 o'clock direction ("upward"),  $\theta_{\phi=180}$  ( $=\theta_9$ ) as the 9 o'clock direction ("left") and  $\theta_{\phi=270}$  ( $=\theta_6$ ) as the 6 o'clock direction ("bottom"). While scanning  $\theta$  and/or  $\phi$ , the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 12.0V  $\pm$ 10% at  $25^{\circ}\text{C}$ . Optimum viewing angle direction is 6 'clock.

< Table 15. Optical Table >

[VDD = 12.0V, Frame rate = 60Hz, Ta =  $25\pm 2^{\circ}\text{C}$ ]

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	$\Theta_3$	CR > 10	-	89	-	Deg.	-
		$\Theta_9$		-	89	-	Deg.	
	Vertical	$\Theta_{12}$		-	89	-	Deg.	
		$\Theta_6$		-	89	-	Deg.	
Contrast ratio		CR		1000:1	1200:1	-		-
Reproduction of color	White	$W_x$	$\Theta = 0^{\circ}$ (Center) Normal Viewing Angle	TYP. - 0.03	0.280	TYP. + 0.03		Based on BOE Backlight
		$W_y$			0.290			
	Red	$R_x$			0.642			
		$R_y$			0.340			
	Green	$G_x$			0.620			
		$G_y$			0.154			
	Blue	$B_x$			0.057			
		$B_y$						
Response Time	G to G	$T_g$		-	8	10	ms	-
Gamma Scale				2.0	2.2	2.4		
Cell Transmittance				0.9Typ	4.1	-	%	Note 5

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of  $\theta = 0^\circ$  and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See Figure 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in Table 15 shall be calculated from the spectral data measured with all pixels first in red, green, blue. Measurements shall be made at the center of the panel. The BLU is used by BOE.
4. Response time Tg is the average time required for display transition by switching the input signal as below table and is based on Frame rate fV =60Hz to optimize. Each time in below table is defined as Figure 2 and shall be measured by switching the input signal for "any level of gray(bright)"and "any level of gray(dark)"

Measured Response Time	Target																
	0	15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255
0																	
15																	
31																	
47																	
63																	
79																	
95																	
111																	
127																	
143																	
159																	
175																	
191																	
207																	
223																	
239																	
255																	

5. Definition of Transmittance (T%) :

Module is with white(L255) signal input

$$\text{Transmittance} = \frac{\text{Luminance of LCD Module}}{\text{Luminance of BLU}} \times 100 \%$$

## 8.0 MECHANICAL CHARACTERISTICS

### 8.1 Dimensional Requirements

Figure 3(located in Appendix) shows mechanical outlines for the model [DV430QUB-P10](#). Other parameters are shown in Table 16.

< Table 16. Dimensional Parameters >

Parameter	Specification	Unit
Active area	941.184(H) × 529.416 (V)	mm
Pixel pitch	81.7(H) × 245.1 (V)	μm
Number of pixels	3840(H) × 2160(V) (TFT pixel) 3840(H) × 2160(V) (1 CF pixel= R + G + B dots)	pixels

**9.0 RELIABILITY TEST**

The Reliability test items and its conditions are shown in below.

< Table 17. Reliability Test Parameters >

No	Test Items	Conditions
1	High temperature storage test	Ta = 60 °C, 240 hrs
2	Low temperature storage test	Ta = -20 °C, 240 hrs
3	High temperature & high humidity operation test	Ta = 50 °C, 80%RH, 240hrs
4	High temperature operation test	Ta = 50 °C, 240hrs
5	Low temperature operation test	Ta = 0 °C, 240hrs
6	Thermal shock	Ta = -20 °C ↔ 60 °C (0.5 hr), 100 cycle

This test condition is based on BOE module.

## 10.0 HANDLING & CAUTIONS

### (1) Cautions when taking out the Panel

- Pick the pouch only, when taking out panel from a shipping package.

### (2) Cautions for handling the panel

- As the electrostatic discharges may break the LCD panel, handle the LCD panel with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD panel should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD panel is operating.
- Put the panel display side down on a flat horizontal plane.
- Handle connectors and cables with care.

### (3) Cautions for the operation

- When the panel is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the panel would be damaged.

### (4) Cautions for the atmosphere

- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD panel in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

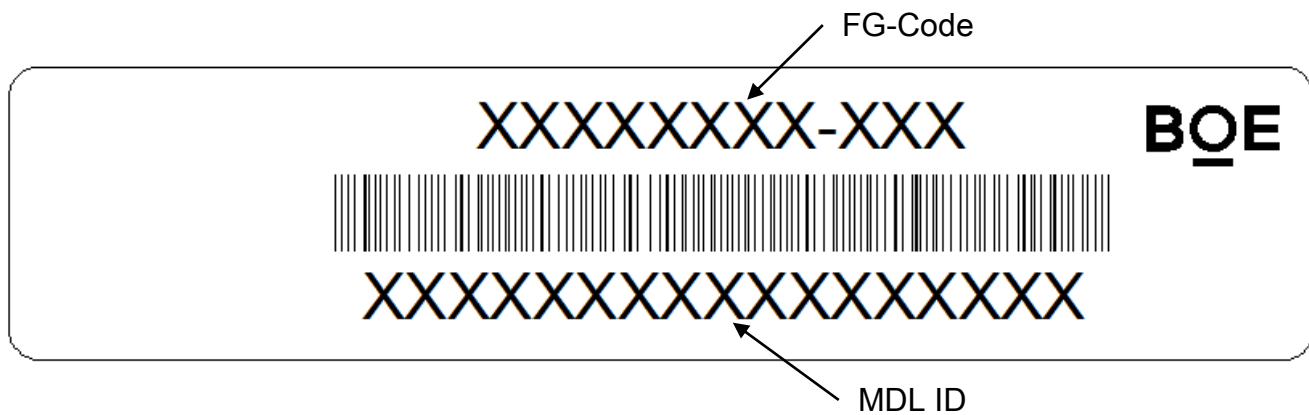
### (5) Cautions for the panel characteristics

- Do not apply fixed pattern data signal to the LCD panel at product aging.
- Applying fixed pattern for a long time may cause image sticking.

### (6) Other cautions

- Do not disassemble and/or re-assemble LCD panel.
- Do not re-adjust variable resistor or switch etc.
- When returning the panel for repair or etc., Please pack the panel not to be broken. We recommend to use the original shipping packages.

### 11.0 PRODUCT SERIAL NUMBER



#### MDL ID Naming Rule:

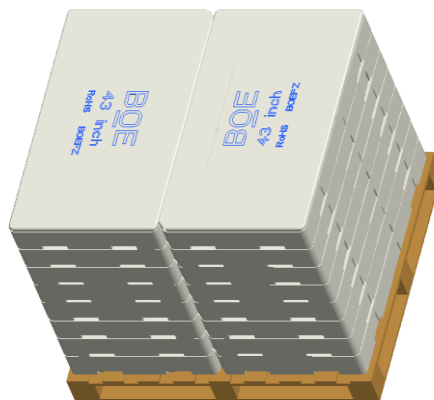
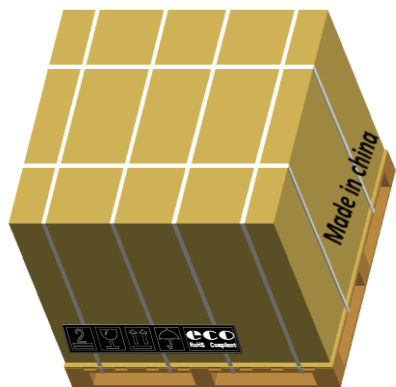
Digit Code	1	2	3	4	5	6	7	8	9	10	11
Description	Model Code GBN		Grade	Line	Year		Month	Model Extension Code			
Digit Code	12	13	14	15	16	17	18				
Description	Serial No						扫码不显示，BOE厂内用				

### 12.0 PACKING

BOE provides the standard shipping container for customers, unless customer specifies their packing information. The standard packing method and Barcode information are shown in below.

#### 12.1 Packing Order

Put 1Pcs EPE Pad in the box, then put 1 Pcs Panel into the box      Totally 17pcs panels and 18Pcs EPE Pad per box



Place wrap film and out box around the boxes. Pack with 6 packing belts.

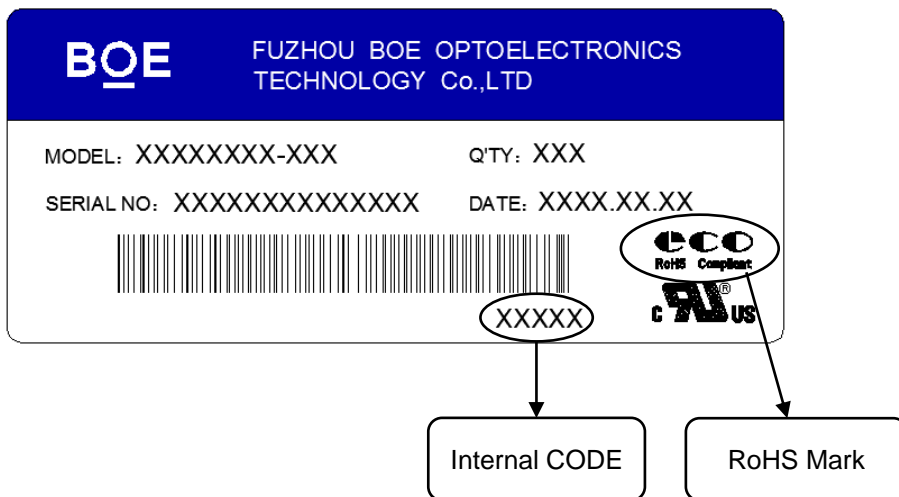
Fix one paper pad on the pallet, Put totally 16 boxes and 2 cover. (16ea boxes per pallet)

### 12.2 Packing Note

- Box Dimension : 1104mmL×706mmW×127mmH
- Package Quantity in one Box : 17pcs

### 12.3 Box Label

- Label Size : 70 mm (L) × 30 mm (W)
- Contents
  - Model : **DV430QUB-P10** ( FG Code of Product )
  - Q`ty : 17 Open Cell in one box.
  - Serial No. : Box Serial No.
  - Date : Packing Date



### Box ID Naming Rule:

Digit Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Description	Products GBN		Grade	Line	Year	Month	Revision Code	Serial No					

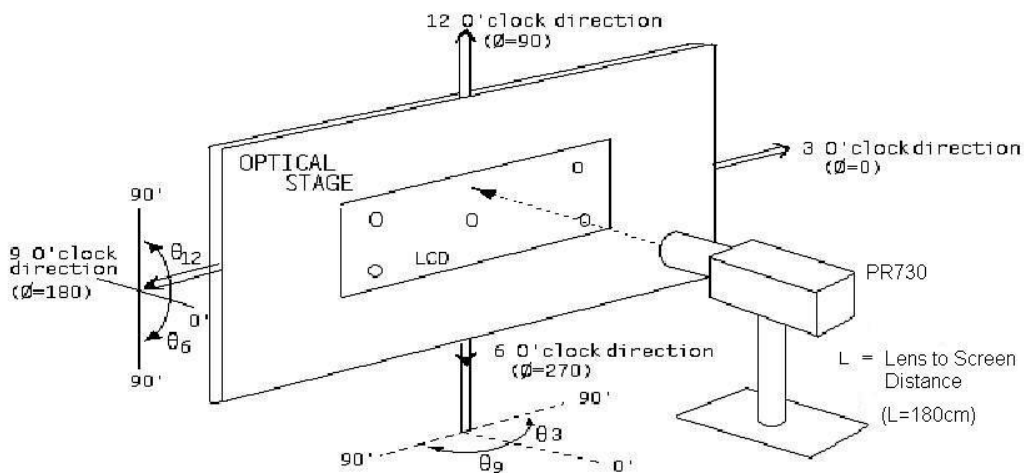
### 12.4 Packing Material ESD Specification

Item	SPEC
Surface Resistance [10 <sup>n</sup> Ω]	Control by 10 <sup>6</sup> ~10 <sup>11</sup> - Box, Spacer, POL Protection film



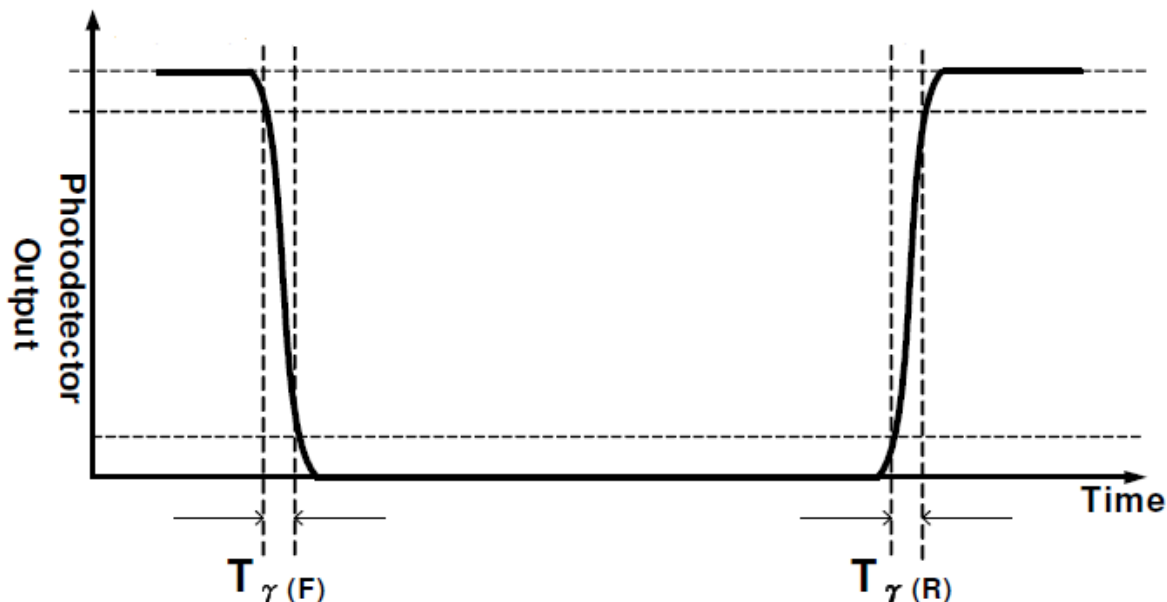
### 13.0 APPENDIX

< Figure 1. Measurement Set Up >



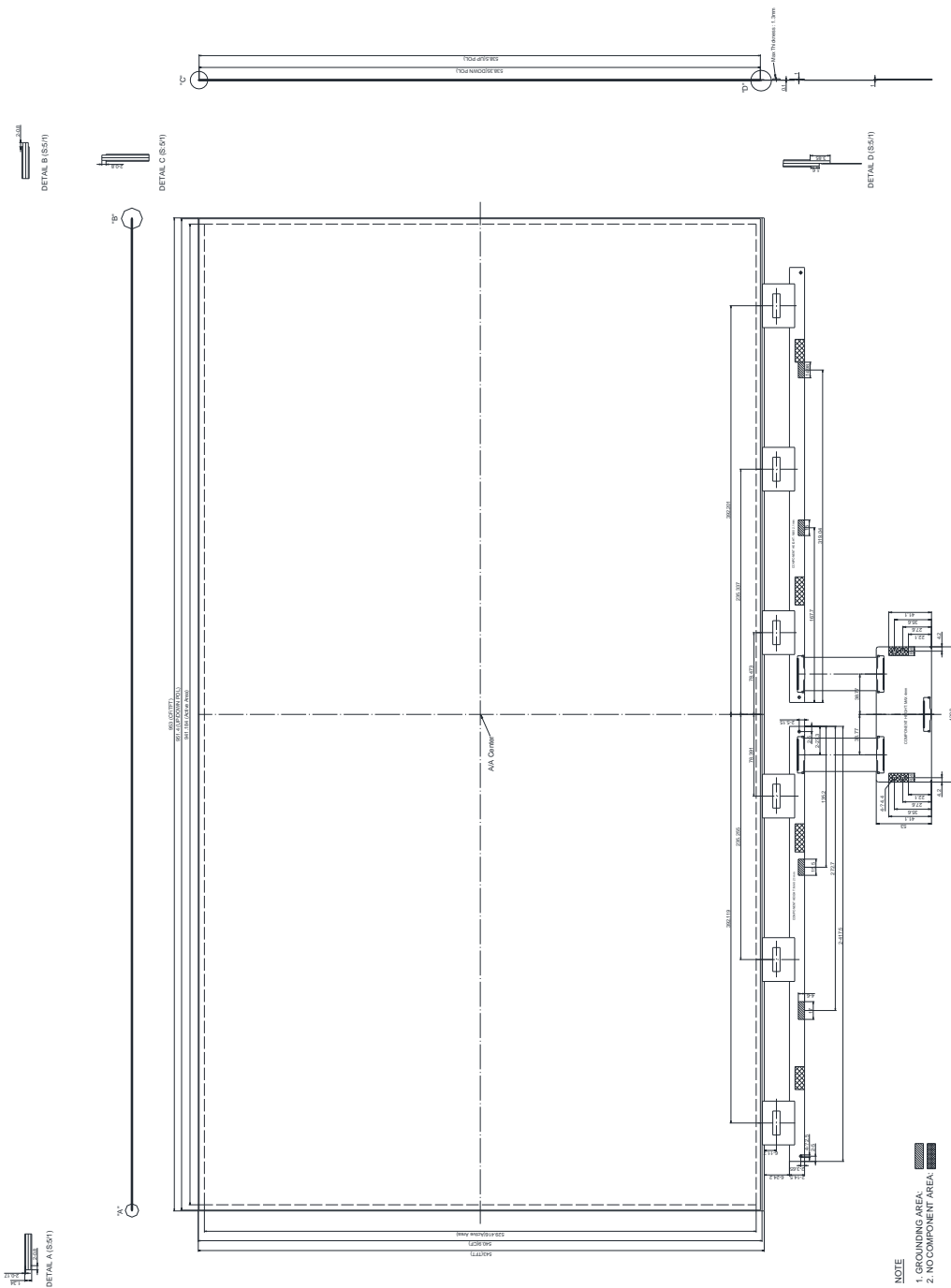
< Figure 2. Response Time Testing >

Any level of gray (Bright)      Any level of gray (Dark)      Any level of gray (Bright)



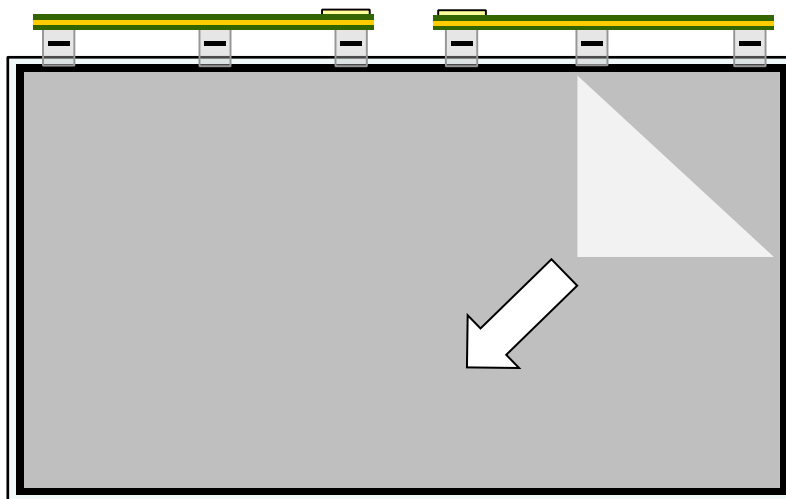
### 13.0 APPENDIX

< Figure 3. TFT-LCD Open Cell Outline Dimensions (Front View) >



## 13.0 APPENDIX

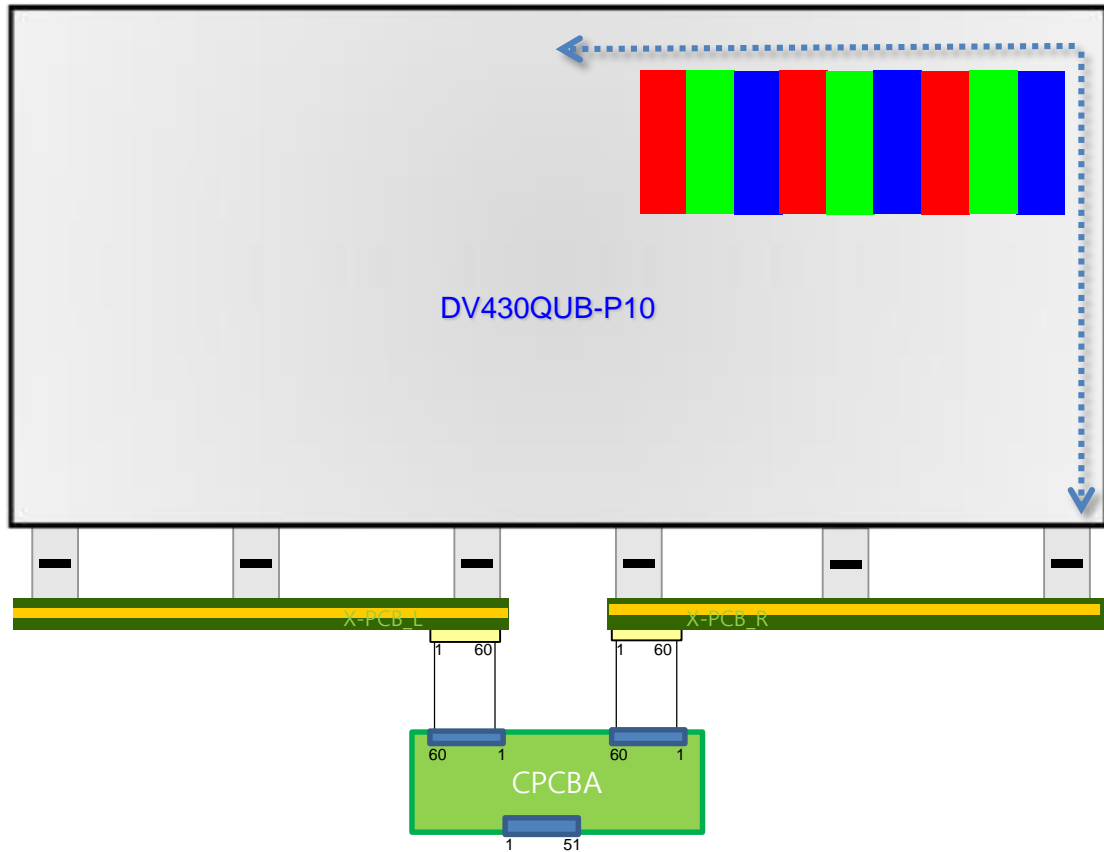
< Figure 4. TFT POL Protect Film Peeling Method >



1. Be sure to peel off slowly(recommended more than 7sec) and constant speed.
2. Peeling direction shows in Figure 4.
3. Be sure to ground person with adequate methods such as the anti-static wrist band.
4. Be sure to ground each S-PCB while peeling off the protection film.
5. Ionized air should be blown over during peeling action.
6. The protection film must not touch drivers and S-PCBs.
7. If adhesive may remain on the polarizer after the protection film peeling off, please remove with isopropyl-alcohol.

**13.0 APPENDIX**

(a) This Product is Reverse type display Mode



1. Panel scan direction is from top to bottom.
2. Driver data latch direction is from right to left.