TITLE : HV110QUB-E10

Open Cell Specification

Rev.A

Fuzhou BOE Optoelectronics Technology Co., Ltd.

REVISION HISTORY

( )Preliminary specification
(√)Final specification

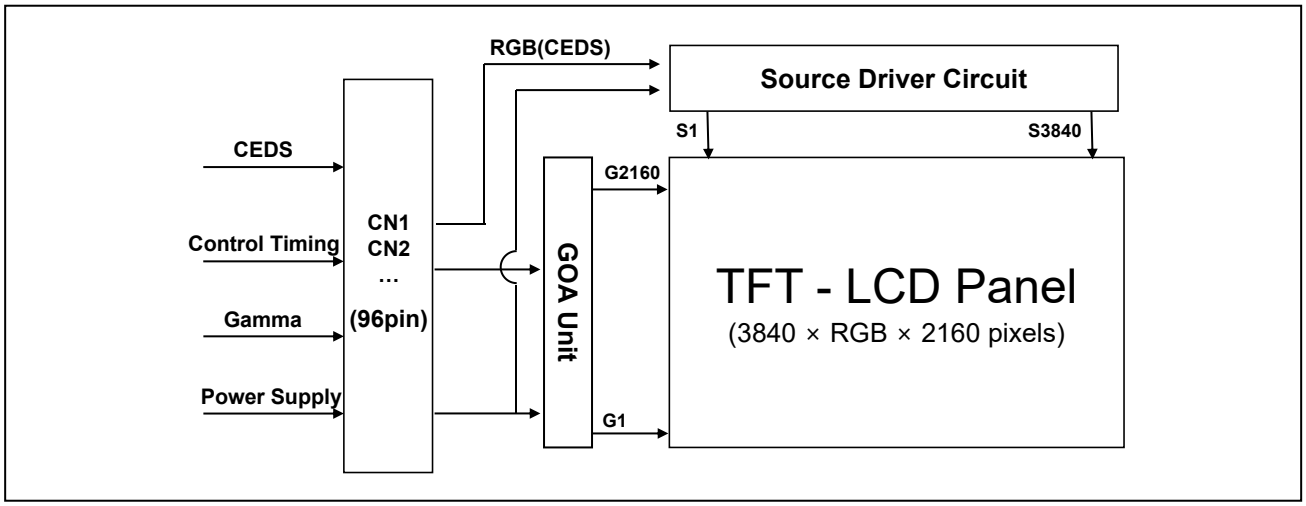
Revision No.	Page	Description of changes	Date	Prepared
P0	All	Initial Release	2024.01.24	Xiu Tianxun
P1	22	Delete HSR Timing: HV110QU-E10 don't support HSR Function	2024.03.07	Xiu Tianxun
P2	7/11/22/ 24/25	Update TBD Spec	2024.04.19	Xiu Tianxun
O	All	Final Release	2024.06.12	Xiu Tianxun
A	5	Update POL Hardness Spec	2024.07.02	Xiu Tianxun

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

HV110QUB-E10 is a color active matrix TFT LCD open cell using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 110 inch diagonally measured active area with UHD resolutions (3840 horizontal by 2160 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in Z-inversion stripe and this module can display 1.07G colors. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.



1.2 Features

- CEDS interface with 24 pairs
- High-speed response
- Low color shift image quality
- 8-bit + FRC color depth, display 1.07G colors
- High luminance and contrast ratio, low reflection and wide viewing angle
- Gate driver use GOA mode
- ADS technology is applied for high display quality
- Support 48~165Hz VRR
- RoHS compliant

1.3 Application

- Home Alone Multimedia TFT-LCD TV only
- Ultra High Definition TV(UHD TV)
- Display Terminals for Control System, Public Monitor and etc… are not allowed

1.4 General Specification

< Table 1. General Specifications >

Parameter	Specification	Unit	Remark
Active area	2436.48(H) × 1370.52(V)	mm	
Number of pixels	RGB：3840*(RGB)*2160	pixels	
Pixel pitch	211.5(H) ×3（RGB）×634.5(V)	μm	
Panel outline	2462.48±0.2（H）x 1388.52±0.2（V) x 1.377±0.1（T）	mm	
Pixel arrangement	Pixels RGB 2G2D Z-inversion stripe	-	
Display colors	1.07G (8bits + FRC)	colors	8bit driver IC
Display mode	Transmission mode, Normally Black		
Open Cell Transmittance	3.8(TYP.)	%	At center point with BOE BLU(YAG With DPP)
Weight	10000(TYP.)	gram	
Power Consumption	20(TYP)/75(MAX)	Watt	With TCON board
Surface Treatment	-Front Polarizer：STW LR, < 9B(GB/T 31378) 2H (LR表涂企业标准/BOE测试标准) -Bottom Polarizer：Clear	-	后续按GB/T 31378管控
Protection Film Peeling Force	20(MAX)	Gf/25 mm	Measured by JIS Z 0327

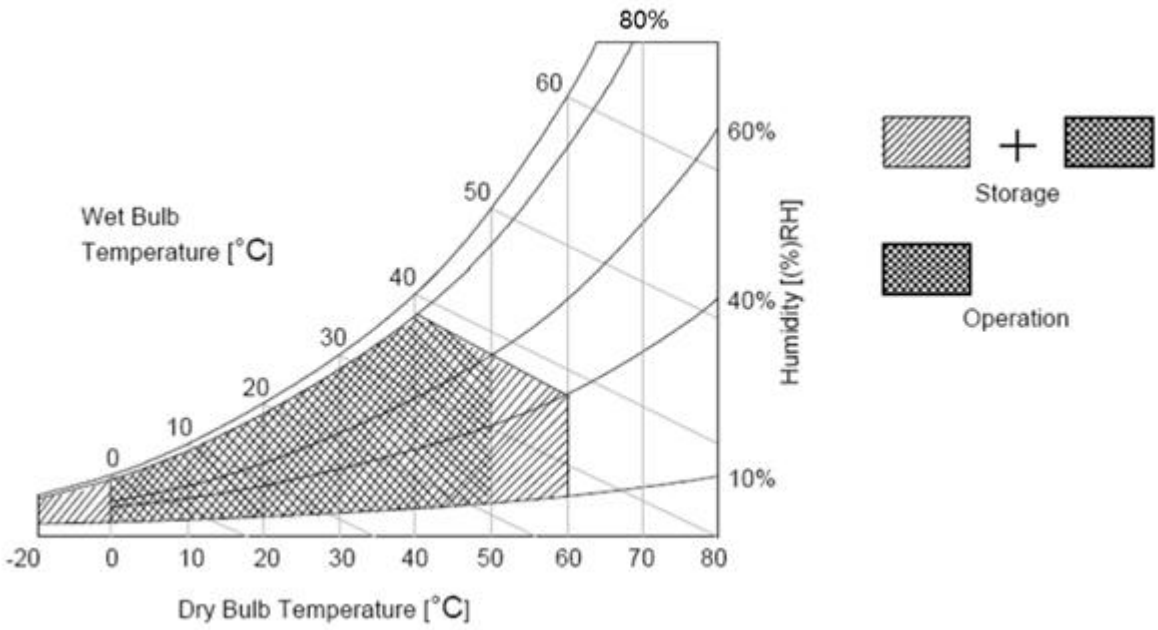
2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum values are listed in the below table.

< Table 2. Open Cell Absolute Maximum Ratings >

Parameter	Symbol	Min.	Max.	Unit	Remark
Operating Temperature	T_{OP}	0	+50	℃	Note 1
	T_{SUR}	0	+60	℃	
Storage Temperature	T_{ST}	-20	+60	℃	
Operating Ambient Humidity	Hop	10	80	%RH	
Storage Humidity	Hst	10	80	%RH	

Note 1 : Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 ℃ max. and no condensation of water.



3.0 ELECTRICAL SPECIFICATIONS

3.1 Open Cell Electrical Specifications

< Table 3. Open Cell Voltage Setting Specifications > [Ta =25±2 ℃]

Characteristics	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	VSS	-8.1	-8	-7.9	V
DC Supply Voltage	LVSS	-10.1	-10	-9.9	V
DC Supply Voltage	VGH	33.5	34	34.5	V
DC Supply Voltage	DVDD1V8S	1.89	1.91	1.98	V
DC Supply Voltage	DVDD1V9S	1.98	2.00	2.05	V
DC Supply Voltage	DVDD3V3	3.2	3.3	3.4	V
DC Supply Voltage	VCOM0	7.2	7.3	7.4	V
DC Supply Voltage	HAVDD	8.5	8.6	8.7	V
DC Supply Voltage	AVDDS	17.5	17.6	17.7	V
DC Supply Voltage	GMA1	16.9	17	17.1	V
DC Supply Voltage	GMA3	15.2	15.3	15.4	V
DC Supply Voltage	GMA5	13.52	13.62	13.72	V
DC Supply Voltage	GMA6	12.39	12.49	12.59	V
DC Supply Voltage	GMA9	8.95	9.05	9.15	V
DC Supply Voltage	GMA10	8.15	8.25	8.35	V
DC Supply Voltage	GMA13	4.81	4.86	4.91	V
DC Supply Voltage	GMA14	3.67	3.72	3.77	V
DC Supply Voltage	GMA16	1.96	2.01	2.06	V
DC Supply Voltage	GMA18	0.27	0.3	0.33	V

Notes:
1. VGH should be tested on SOC board or separate power board. High voltage of STV/CLK/VDDODD/VDDEVEN is as same as VGH voltage.
2. Other test points are on source board. Use typical pattern to test.

3.1 Open Cell Electrical Specifications

< Table 4. Open Cell Current Setting Specifications > [Ta =25±2 ℃]

Characteristics	Symbol	Min	Typ	Max	Unit
DC Supply Current	VSS	-	-	30	mA
DC Supply Current	LVSS	-	-	200	mA
DC Supply Current	VGH	-	-	200	mA
DC Supply Current	DVDD1V8S	-	-	200	mA
DC Supply Current	DVDD1V9S	-	-	200	mA
DC Supply Current	DVDD3V3	-	-	100	mA
DC Supply Current	VCOM0	-	-	30	mA
DC Supply Current	HAVDD	-	-	30	mA
DC Supply Current	AVDDS	-	-	3100	mA
DC Supply Current	GMA1	-	-	30	mA
DC Supply Current	GMA3	-	-	30	mA
DC Supply Current	GMA5	-	-	30	mA
DC Supply Current	GMA6	-	-	30	mA
DC Supply Current	GMA9	-	-	30	mA
DC Supply Current	GMA10	-	-	30	mA
DC Supply Current	GMA13	-	-	30	mA
DC Supply Current	GMA14	-	-	30	mA
DC Supply Current	GMA16	-	-	30	mA
DC Supply Current	GMA18	-	-	30	mA

Notes:
1. Max current is RMS value test with TCON board. When design SOC board or power supply board, the current output capability must more than the maximum current value.
2. Current is RMS value test with TCON board; The input current drive capability must more than the Max value.
3. VCOM short-circuit current is 400mA.
4. VGH should be tested on SOC board or separate power board.
5. Other test points are on SOC board or separate power board. Use maximum pattern to test.

3.1 Open Cell Electrical Specifications

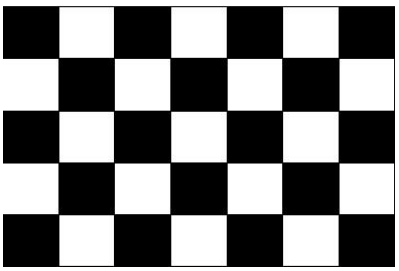
< Table 5. Open Cell Voltage Ripple Specifications > [Ta =25±2 ℃]

Characteristics	Symbol	Max	Unit
DC Supply Ripple	VSS	100	mV
DC Supply Ripple	LVSS	220	mV
DC Supply Ripple	VGH	450	mV
DC Supply Ripple	DVDD1V8S	70	mV
DC Supply Ripple	DVDD1V9S	70	mV
DC Supply Ripple	DVDD3V3	70	mV
DC Supply Ripple	VCOM0	50	mV
DC Supply Ripple	HAVDD	80	mV
DC Supply Ripple	AVDDS	800	mV
DC Supply Ripple	GMA1	150	mV
DC Supply Ripple	GMA3	150	mV
DC Supply Ripple	GMA5	150	mV
DC Supply Ripple	GMA6	100	mV
DC Supply Ripple	GMA9	100	mV
DC Supply Ripple	GMA10	100	mV
DC Supply Ripple	GMA13	100	mV
DC Supply Ripple	GMA14	100	mV
DC Supply Ripple	GMA16	100	mV
DC Supply Ripple	GMA18	50	mV

Notes:
1. Voltage ripple is Vpeak to Vpeak value. The ripple include V-blanking area ripple.
2. VGH should be tested on SOC board or separate power board.
3. Other test points are on source board. Use maximum pattern to test.

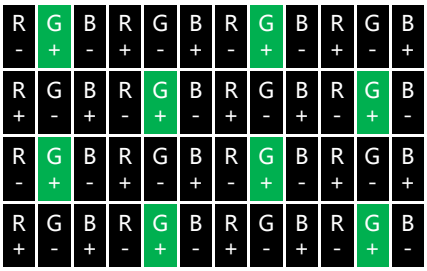
3.2 Power Consumption and Flicker Pattern

a) Typ : Mosaic 7X5 (L0/L255)



b) Max : Horizontal 2 Line(L0/L255)

c) Flicker Test Pattern



3.3 Driver Characteristics

< Table 6. Driver Characteristics >

Parameter	Symbol	Values			Unit	Remark
		Min	Typ	Max		
Driver Surface Temperature	T_{DS}	-	-	125	℃	Note1

Note 1. Any point on the driver surface must be less than 125 ℃ under any conditions.
2. This test condition is based on BOE module.

4.0 OPTICAL SPECIFICATION

The test of optical specifications shall be measured in a dark room (ambient luminance≤1 lux and temperature=25±2℃) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 180cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to $\theta_{Ø=0}$ (=θ_3) as the 3 o'clock direction (the "right"), $\theta_{Ø=90}$ (= θ_{12}) as the 12 o'clock direction ("upward"), $\theta_{Ø=180}$ (= θ_9) as the 9 o'clock direction ("left") and $\theta_{Ø=270}$(= θ_6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 12.0V +/-10% at 25°C. Optimum viewing angle direction is 6 'clock.

< Table 7. Optical Table >

[VDD = 12.0V, Frame rate = 165Hz, Ta =25±2 ℃]

Parameter		Symbol	Condition		Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	Θ_3	CR > 10		-	89	-	Deg.	Note1
		Θ_9			-	89	-	Deg.	
	Vertical	Θ_{12}			-	89	-	Deg.	
		Θ_6			-	89	-	Deg.	
Contrast ratio		CR	Θ = 0° (Center) Normal Viewing Angle		2000	2300	-		Note2
Reproduction of color	White	W_x			TYP. - 0.03	0.250	TYP. + 0.03		Note3
		W_y				0.248			
	Red	R_x				0.646			
		R_y				0.343			
	Green	G_x				0.294			
		G_y				0.637			
	Blue	B_x				0.153			
		B_y				0.035			
Response Time	G to G	T_g	PNL SURF TEMP	25℃	-	6	8	ms	Note4
				5℃	-	28	35		
Cell Transmittance					0.9Typ	3.8	-	%	Note5
Gamma Scale					2.0	2.2	2.4		

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of $\theta = 0°$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See Figure 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in this table shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel. The chromaticity coordinates are based on BOE backlight(YAG With DPP).
4. Response time Tg is the average time required for display transition by switching the input signal as below table and is based on Frame rate fV = 165Hz with BOE Tcon Board to optimize. Each time in below table shall be measured by switching the input signal for "any level of gray(bright)"and "any level of gray(dark)"

Measured Response Time		Target																
		0	15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255
Start	0																	
	15																	
	31																	
	47																	
	63																	
	79																	
	95																	
	111																	
	127																	
	143																	
	159																	
	175																	
	191																	
	207																	
	223																	
	239																	
	255																	

5. Definition of Transmittance (T%) :
   Module is with white(L255) signal input

$$\text{Transmittance} = \frac{\text{Luminance of LCD Module}}{\text{Luminance of BLU}} \times 100\ \%$$

5.0 INTERFACE CONNECTION

5.1 Connector Pin Configuration

< Table 8. Open Cell XPCBL Input Connector Pin Configuration >

P/N	Name
1	FB3
2	GMA18
3	GMA16
4	GMA14
5	GMA13
6	GMA10
7	GMA9
8	GMA6
9	GMA5
10	GMA3
11	GMA1
12	NC
13	LOCKOUT24
14	GND
15	CEDS24B
16	CEDS24A
17	GND
18	CEDS23B
19	CEDS23A
20	GND
21	CEDS22B
22	CEDS22A
23	GND
24	CEDS21B
25	CEDS21A
26	GND
27	CEDS20B
28	CEDS20A
29	GND
30	CEDS19B
31	CEDS19A
32	GND
33	CEDS18B
34	CEDS18A
35	GND
36	CEDS17B
37	CEDS17A
38	GND
39	CEDS16B
40	CEDS16A

P/N	Name
41	GND
42	CEDS15B
43	CEDS15A
44	GND
45	CEDS14B
46	CEDS14A
47	GND
48	CEDS13B
49	CEDS13A
50	GND
51	LOCKOUT12
52	VTERM(NC)
53	GND
54	DVDD1V8S
55	DVDD1V8S
56	DVDD1V9S
57	DVDD1V9S
58	NC
59	HAVDD
60	HAVDD
61	AVDD
62	AVDD
63	AVDD
64	AVDD
65	AVDD
66	VCOM_IN
67	VCOM_IN
68	GND
69	NC
70	NC
71	NC
72	NC
73	NC
74	GND
75	LVSS
76	VSS
77	GND
78	NC
79	STV1
80	STV0

P/N	Name
81	VDDE
82	VDDO
83	GND
84	NC
85	NC
86	CLK10
87	CLK9
88	CLK8
89	CLK7
90	CLK6
91	CLK5
92	CLK4
93	CLK3
94	CLK2
95	CLK1
96	FB2

5.1 Connector Pin Configuration

< Table 9. Open Cell XPCBR Input Connector Pin Configuration >

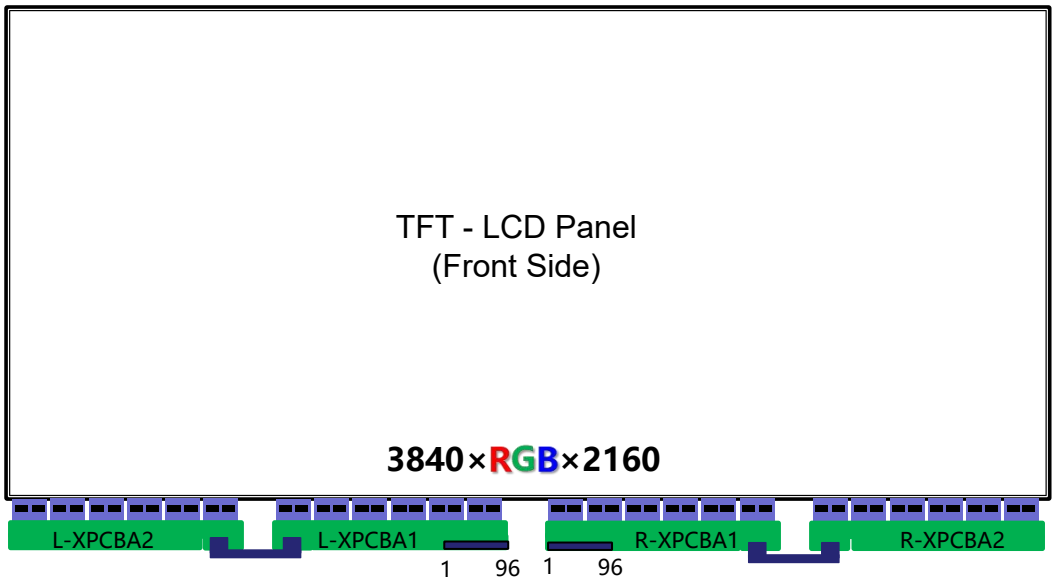
P/N	Name
1	FB2
2	CLK1
3	CLK2
4	CLK3
5	CLK4
6	CLK5
7	CLK6
8	CLK7
9	CLK8
10	CLK9
11	CLK10
12	NC
13	NC
14	GND
15	VDDODD
16	VDDEVEN
17	STV0
18	STV1
19	NC
20	GND
21	VSS
22	LVSS
23	GND
24	DM_CS
25	DM_DO
26	DM_SCK
27	DM_DI
28	DVDDS_3V3
29	GND
30	VCOM_IN
31	VCOM_IN
32	AVDD
33	AVDD
34	AVDD
35	AVDD
36	AVDD
37	HAVDD
38	HAVDD
39	NC
40	DVDD1V9S

P/N	Name
41	DVDD1V9S
42	DVDD1V8S
43	DVDD1V8S
44	GND
45	VTERM(NC)
46	LOCKOUT12
47	GND
48	CEDS12B
49	CEDS12A
50	GND
51	CEDS11B
52	CEDS11A
53	GND
54	CEDS10B
55	CEDS10A
56	GND
57	CEDS9B
58	CEDS9A
59	GND
60	CEDS8B
61	CEDS8A
62	GND
63	CEDS7B
64	CEDS7A
65	GND
66	CEDS6B
67	CEDS6A
68	GND
69	CEDS5B
70	CEDS5A
71	GND
72	CEDS4B
73	CEDS4A
74	GND
75	CEDS3B
76	CEDS3A
77	GND
78	CEDS2B
79	CEDS2A
80	GND

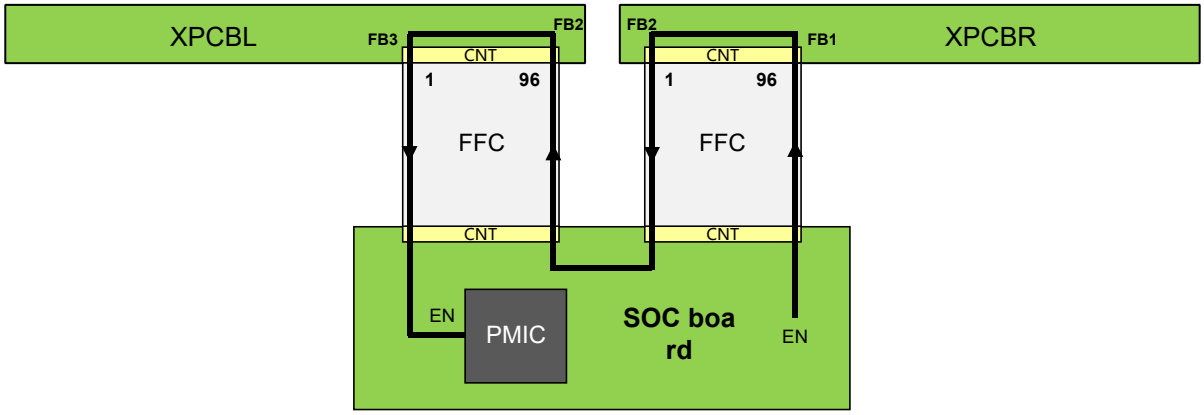
P/N	Name
81	CEDS1B
82	CEDS1A
83	GND
84	NC
85	GND
86	GMA18
87	GMA16
88	GMA14
89	GMA13
90	GMA10
91	GMA9
92	GMA6
93	GMA5
94	GMA3
95	GMA1
96	FB1

Notes :

1. NC (Not Connected) : These pins show status of T/con board and are only used for BOE internal operations.
2. XPCBL and XPCBR Input pins assignments refer to the below diagram.



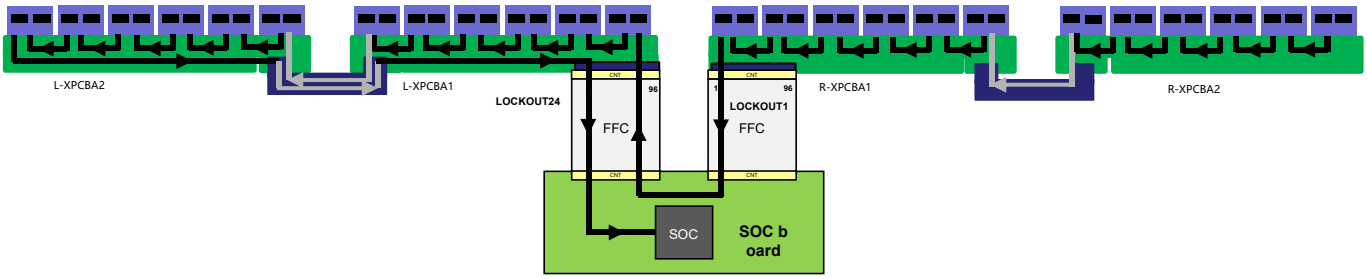
3. FB3/2/1 are used for FB function. Aim to avoid electrical damage when FFC skew plug happens. When using FB function, it requires customers to design circuit and power supply sequence which depends on power IC on SOC board. Otherwise, ignore FB function and keep these pins NC.



4. VTERM pin is used for CEDS CML mode only. This product supports LVDS mode Only. Keep this pin NC when using LVDS mode.

Notes :

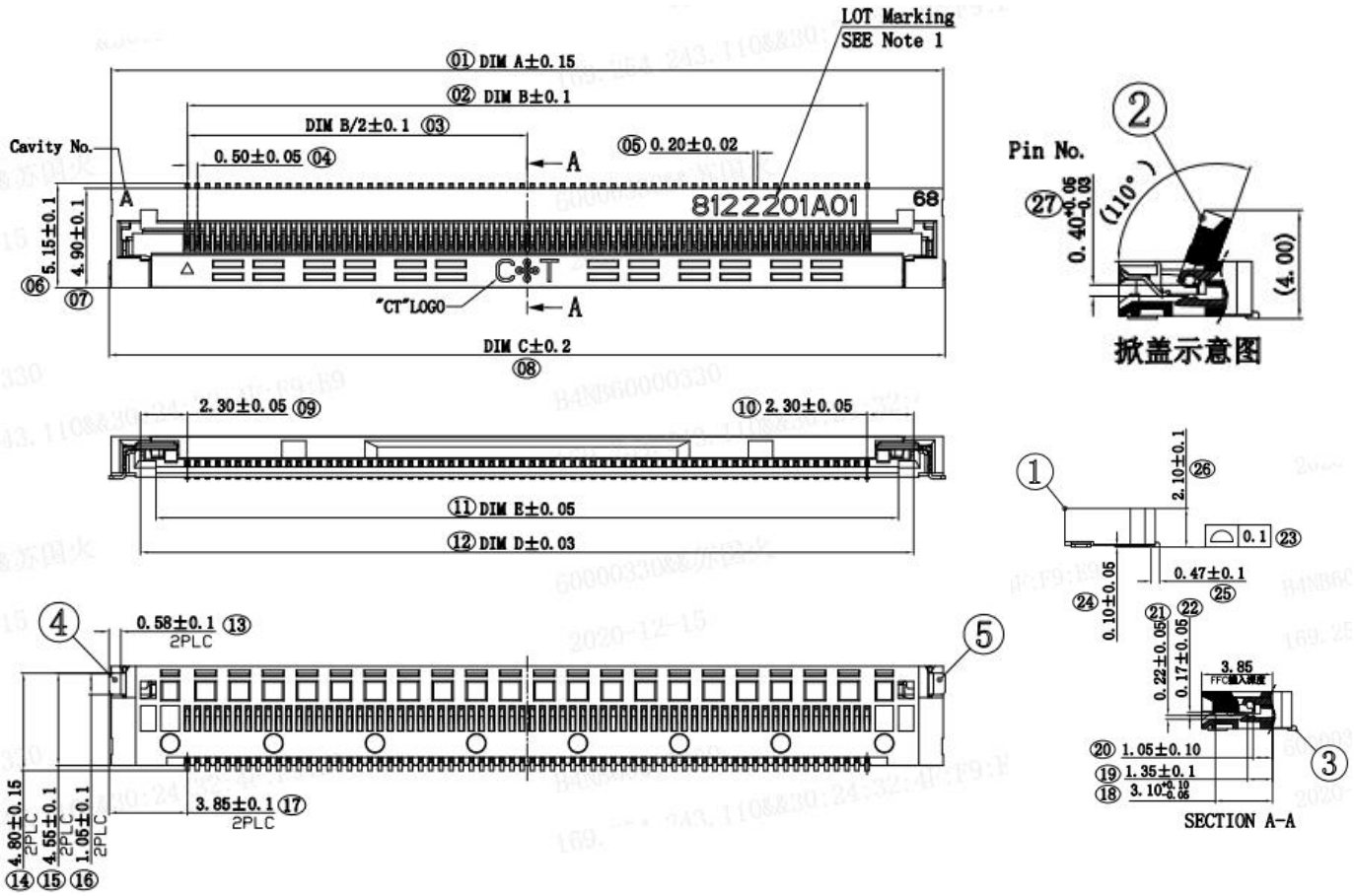
5. LOCKOUT1-24 are CEDS driver IC internal check signal. It will be pull low to ground voltage when driver IC has abnormal state. If LOCK signal receiver detect low voltage, the receiver has to resend CEDS training signal until all drivers locked normally. Then last LOCK signal is continuous high voltage 1.8V. Refer to the below diagram.



5.0 INTERFACE CONNECTION

5.2 Open Cell Input Connector & FFC Drawing

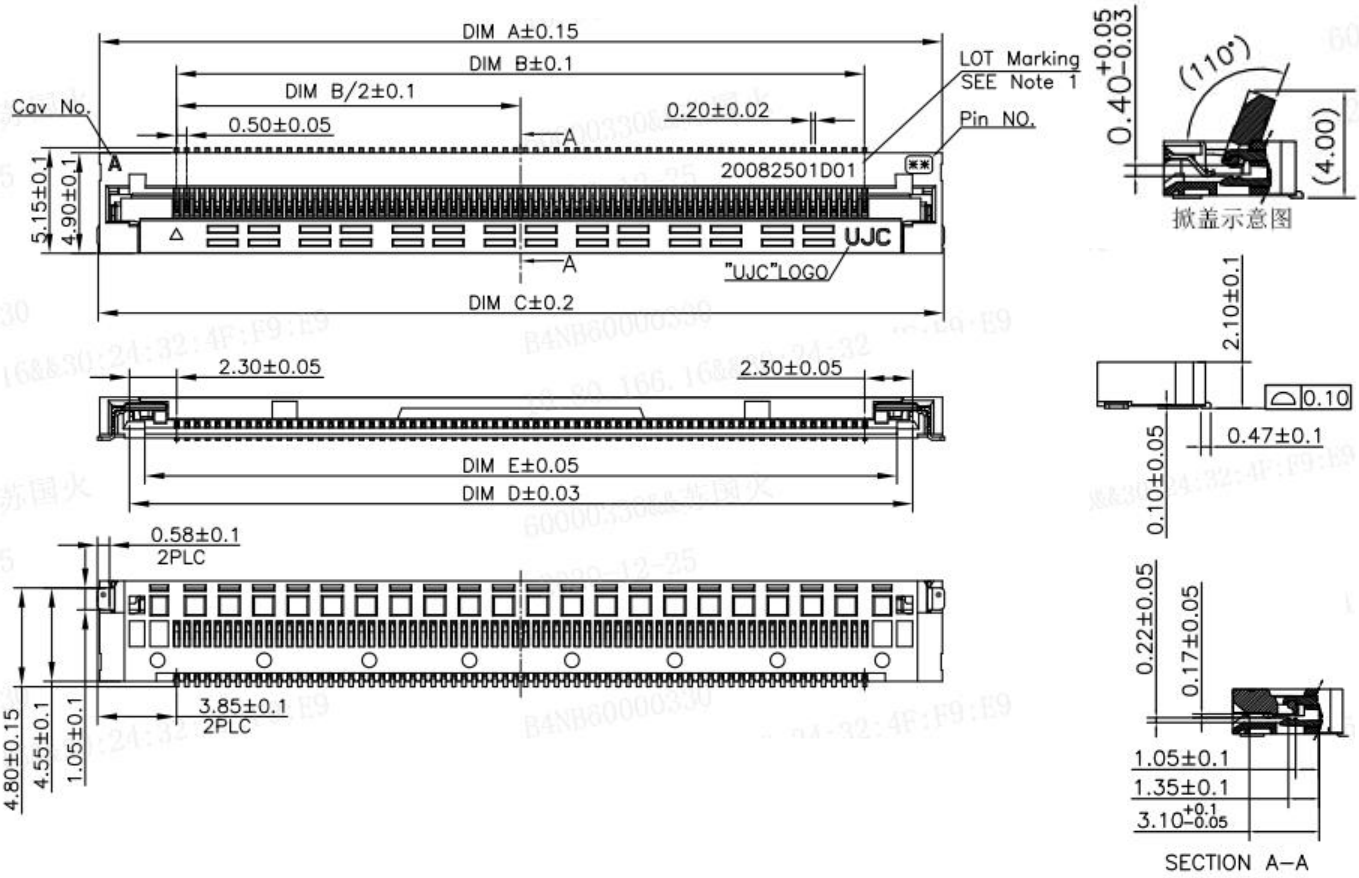
-96pin Connector Drawing-F05049-96P-H



PIN NO.	DIM A	DIM B	DIM C	DIM D	DIM E
96	55.00	47.50	55.20	52.10	50.60

5.2 Open Cell Input Connector & FFC Drawing

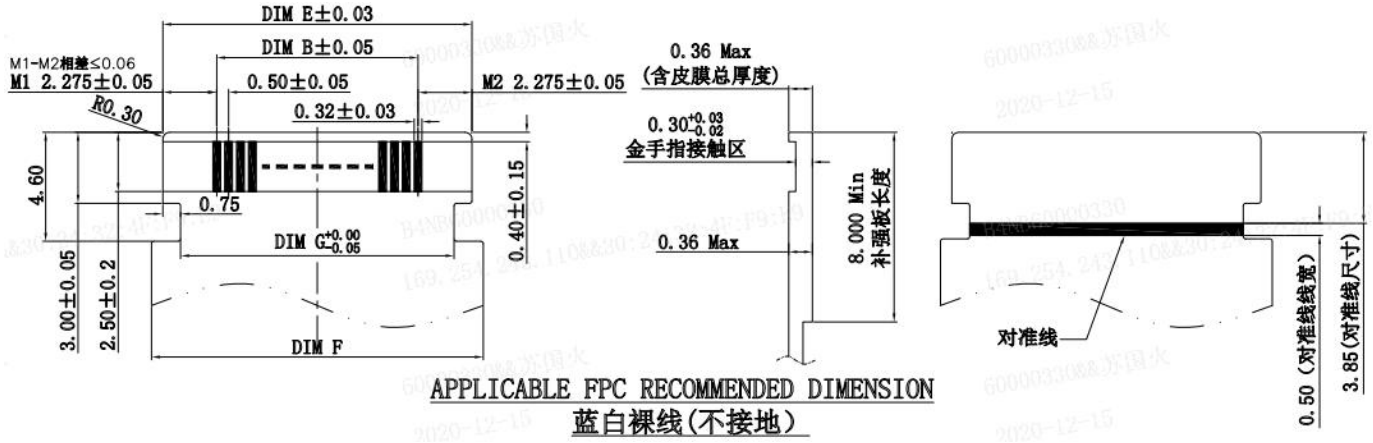
-96pin Connector Drawing-PM.FPC.LVS4909601



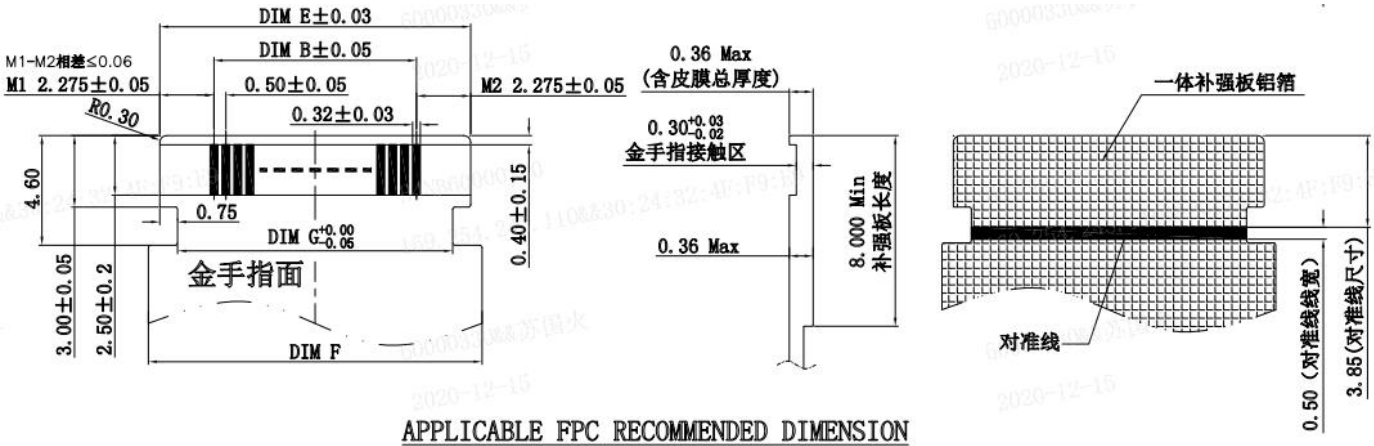
PIN NO.	DIM A	DIM B	DIM C	DIM D	DIM E
96	55.00	47.50	55.20	52.10	50.60

5.2 Open Cell Input Connector & FFC Drawing

-96pin FFC Drawing



APPLICABLE FPC RECOMMENDED DIMENSION
蓝白裸线(不接地)



APPLICABLE FPC RECOMMENDED DIMENSION
一体补强板铝箔FFC线

PIN NO.	DIM B	DIM E	DIM F	DIM G
96	47.50	52.05	53.00	50.55

Notes: This FFC drawing is supplied by the connector vendor. It is for reference only.

6.0 INTERFACE SIGNAL TIMING SPECIFICATION

6.1 Signal Timing Parameters

< Table 10. 165Hz Timing Table >

Item		Symbols	Min	Typ	Max	Unit
Pixel Clock Frequency		1/Tc	96	98.38	99.5	MHz
Frame Rate		F	48	165	165	Hz
Vertical	Total	T_V	2200	2250	7734	T_H
	Display	T_{VD}	2160			T_H
	Blank	T_{VB}	40	90	5574	T_H
Horizontal	Total	T_H	260	265	270	T_{CLK}
	Display	T_{HD}	240			T_{CLK}
	Blank	T_{HB}	20	25	30	T_{CLK}

Notes:

1.This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

2. This product should keep clock frequency and Horizontal value fixed when adjusting frame rate.

3. It is recommended that the PWM frequency should be an integer multiple of the frame rate , If BLU use PWM mode.

6.0 INTERFACE SIGNAL TIMING SPECIFICATION

6.1 Signal Timing Parameters

< Table 11. 144Hz/120Hz Timing Table >

Item		Symbols	Min	Typ	Max	Unit
Pixel Clock Frequency		1/Tc	84	85.86	87.5	MHz
Frame Rate		F	48	144	144	Hz
Vertical	Total	T_V	2200	2250	6750	T_H
	Display	T_{VD}	2160			T_H
	Blank	T_{VB}	40	90	4590	T_H
Horizontal	Total	T_H	260	265	275	T_{CLK}
	Display	T_{HD}	240			T_{CLK}
	Blank	T_{HB}	20	25	35	T_{CLK}

Item		Symbols	Min	Typ	Max	Unit
Pixel Clock Frequency		1/Tc	69	74.25	77	MHz
Frame Rate		F	48	120	122	Hz
Vertical	Total	T_V	2200	2250	5625	T_H
	Display	T_{VD}	2160			T_H
	Blank	T_{VB}	40	90	3465	T_H
Horizontal	Total	T_H	270	275	280	T_{CLK}
	Display	T_{HD}	240			T_{CLK}
	Blank	T_{HB}	30	35	40	T_{CLK}

Notes:

1.This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

2. This product should keep clock frequency and Horizontal value fixed when adjusting frame rate.

3. It is recommended that the PWM frequency should be an integer multiple of the frame rate , If BLU use PWM mode.

6.0 INTERFACE SIGNAL TIMING SPECIFICATION

6.1 Signal Timing Parameters

< Table 12. Real 60Hz Timing Table >

Item		Symbols	Min	Typ	Max	Unit
Pixel Clock Frequency		1/Tc	69	74.25	77	MHz
Frame Rate		F	47	60(50)	62	Hz
Vertical	Total	T_V	2200	2250(2700)	2872	T_H
	Display	T_{VD}	2160			T_H
	Blank	T_{VB}	40	90(540)	712	T_H
Horizontal	Total	T_H	530	550	570	T_{CLK}
	Display	T_{HD}	480			T_{CLK}
	Blank	T_{HB}	50	70	90	T_{CLK}

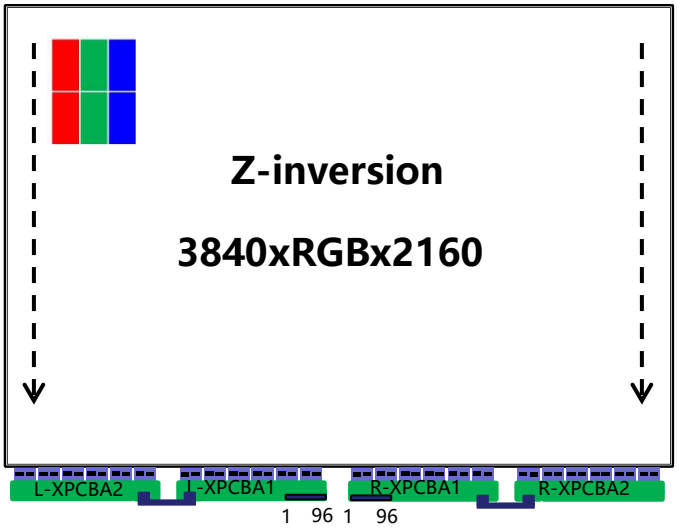
Notes:

1.This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

2. This product should keep clock frequency and Horizontal value fixed when adjusting frame rate.

3. It is recommended that the PWM frequency should be an integer multiple of the frame rate , If BLU use PWM mode.

6.2 Pixel Structure

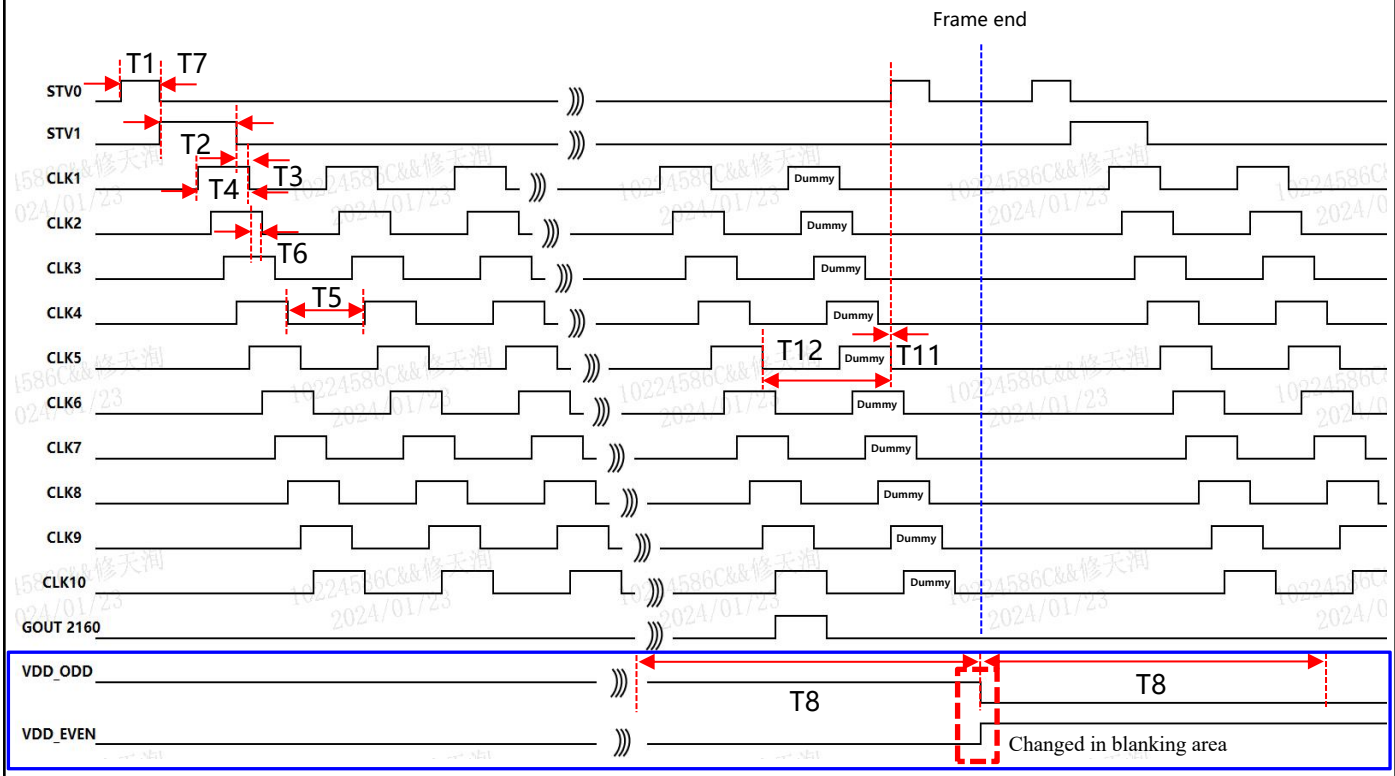


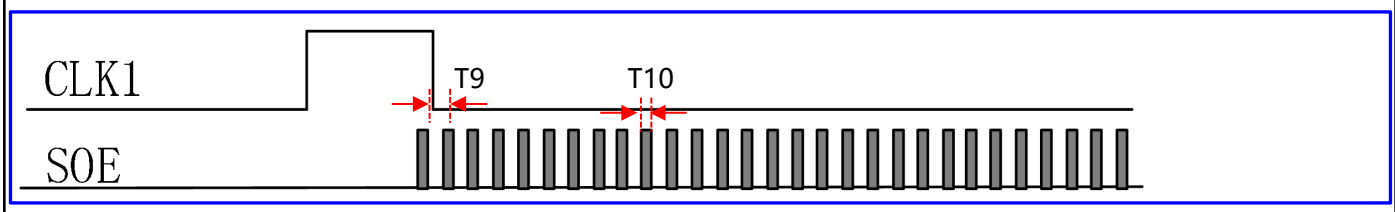
Notes:

1. Panel is progressive scan from top to bottom.
2. Source driver data latch direction is from right to left.

6.3 Signal Timing Waveform

H total :4400
V total :2250
Frame Rate:60Hz





6.3 Signal Timing Waveform

H total :4400
V total :2250
Frame Rate:60Hz

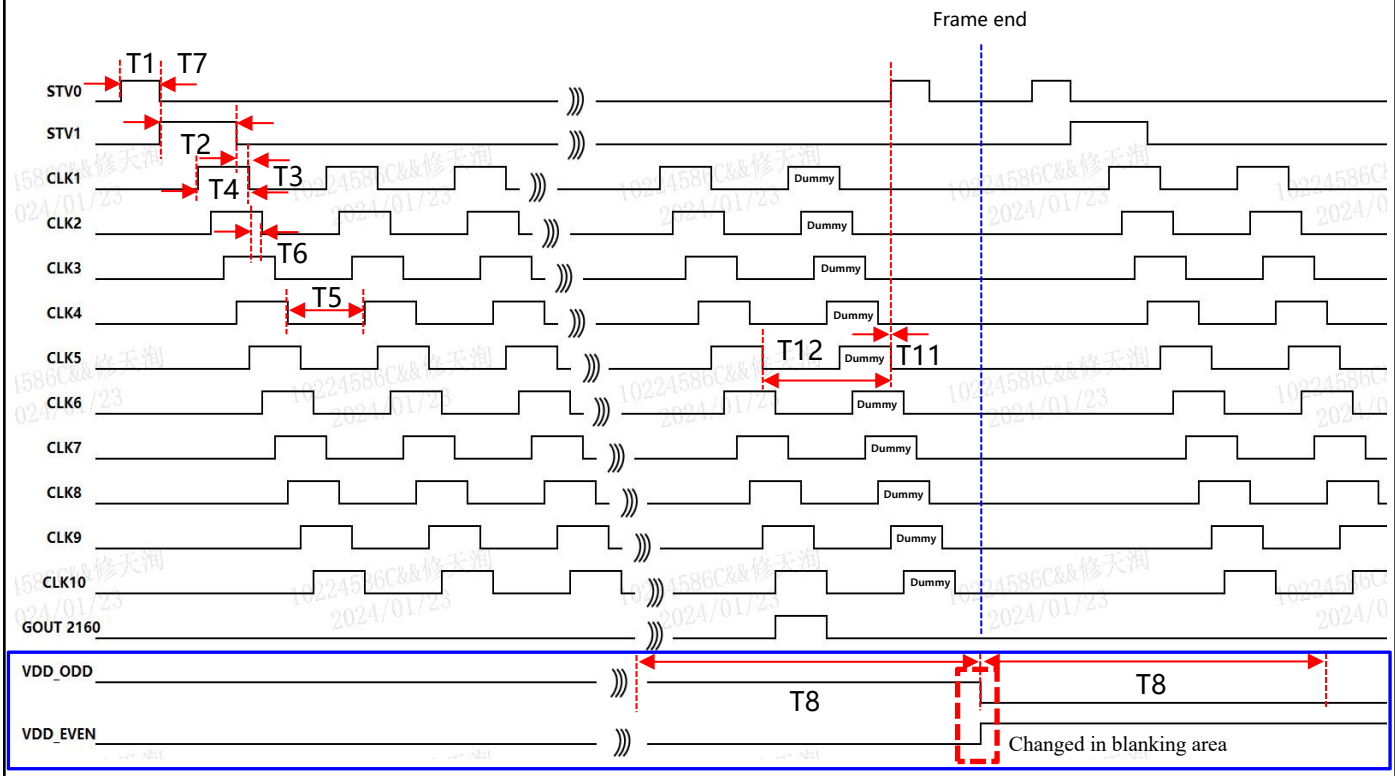
	Min.	Typ.	Max.	Description	Remark
T1	44.2us	44.4us	44.6us	STV0 Width(3H)	
T2	88.6us	88.8us	89us	STV1 Width(6H)	
T3	14.7us	14.8us	14.9us	STV1 Falling to CLK Falling(1H)	
T4	59us	59.2us	59.4us	CLK High Width(4H)	
T5	88.6us	88.8us	89us	CLK Low Width(6H)	
T6	14.7us	14.8us	14.9us	CLK1 Falling to CLK2 Falling(1H)	
T7	0	0	0	STV0 Falling to STV1 Rising	
T8	-	2s	3s	VDDODD/EVEN Changing Period (1 Period of High or Low)	Changed in blanking area
T9	2.9	3.0	3.05	GOE	
T10	-	Refer to CE DS CMD	-	SOE Width	
T11	0	0	7.4us	Dummy CLK5 Falling to STV0 Rising	
T12	147us	148us	149us	Dummy CLK1-10 Keep 1 CLK Period	

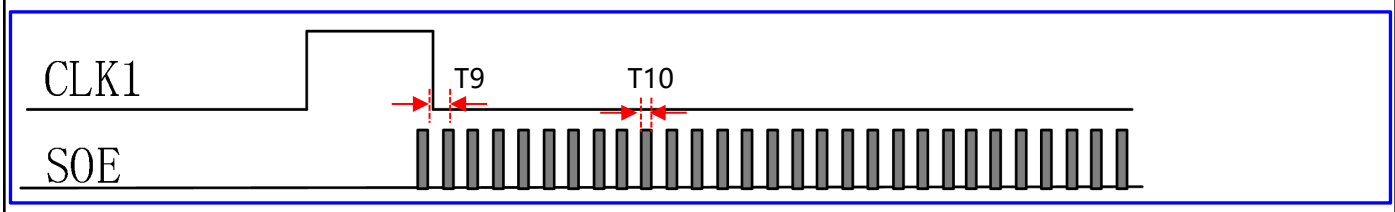
Notes:

1. 1H=14.8us.
2. CLK2~CLK10 High Width is T4, same as CLK1.
3. CLK2~CLK10 Low Width is T5, same as CLK1.
4. CLK2 falling to CLK3 falling, CLK3 falling to CLK4 falling, CLK4 falling to CLK5 falling, CLK5 falling to CL K6 falling, CLK6 falling to CLK7 falling, CLK7 falling to CLK8 falling, CLK8 falling to CLK9 falling, CLK9 fa lling to CLK10 falling, are all T6.
5. When power on, STV0/1 and CLK1~CLK10 should keep low before the first STV0/1.
6. VDDODD and VDDEVEN must reverse in vertical blanking time.
7. Charging sharing function should be set up to by frame.
8. CLK1-10 Keep Dummy CLK 1 CLK Period.
9. VDDODD/VDDEVEN Keep Half Period VGH and Half Period VGL in 1 Period.

6.3 Signal Timing Waveform

H total :4400
V total :2250
Frame Rate:120Hz





6.3 Signal Timing Waveform

H total :4400
V total :2250
Frame Rate:120Hz

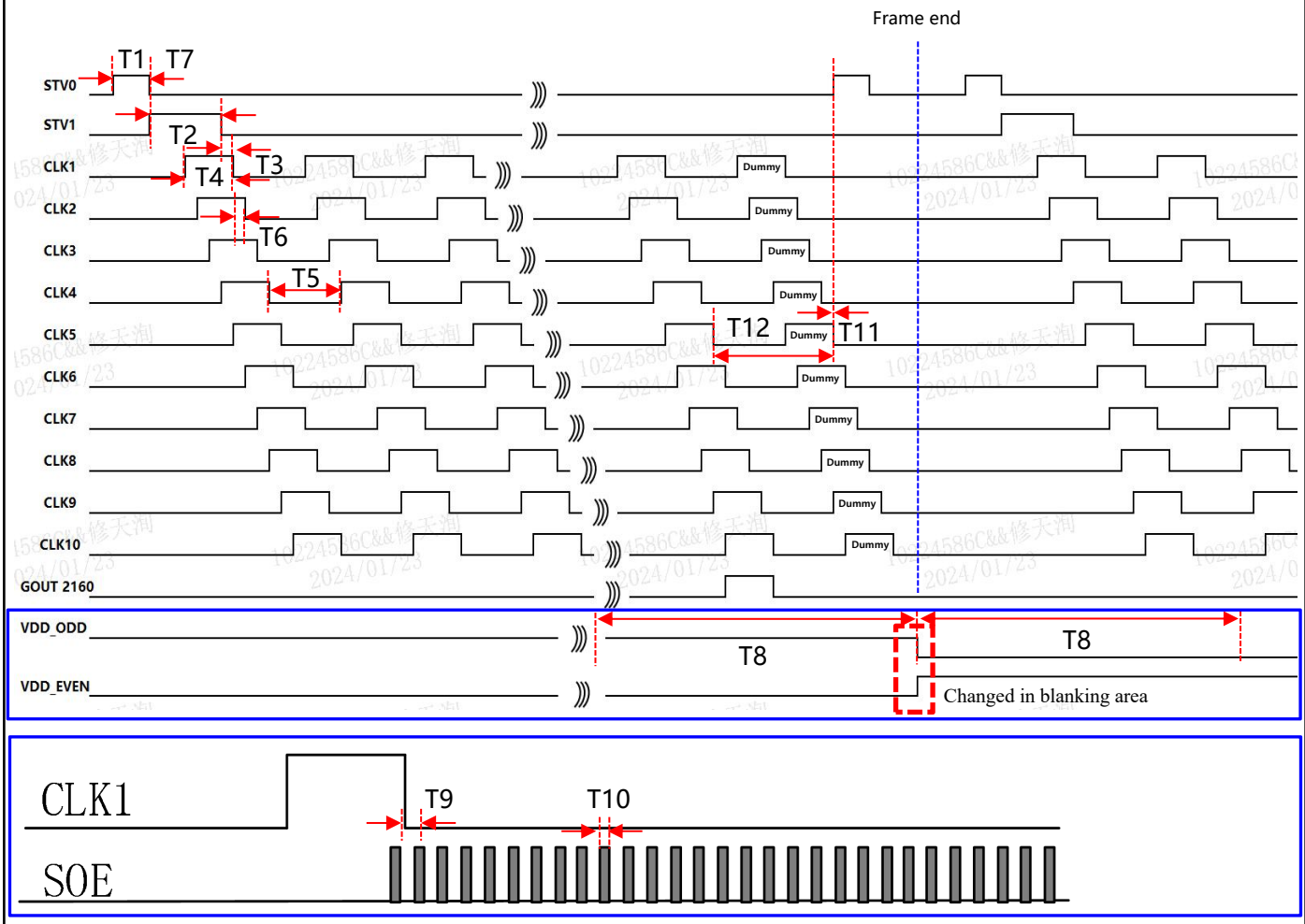
	Min.	Typ.	Max.	Description	Remark
T1	22.1us	22.2us	22.3us	STV0 Width(3H)	
T2	44.3us	44.4us	44.5us	STV1 Width(6H)	
T3	7.35us	7.4us	7.45us	STV1 Falling to CLK Falling(1H)	
T4	29.5us	29.6us	29.7us	CLK High Width(4H)	
T5	44.3us	44.4us	44.5us	CLK Low Width(6H)	
T6	7.35us	7.4us	7.45us	CLK1 Falling to CLK2 Falling(1H)	
T7	0	0	0	STV0 Falling to STV1 Rising	
T8	-	2s	3s	VDDODD/EVEN Changing Period (1 Period of High or Low)	Changed in blanking area
T9	2.9	3.0	3.05	GOE	
T10	-	Refer to CE DS CMD	-	SOE Width	
T11	0	0	7.4us	Dummy CLK5 Falling to STV0 Rising	
T12	73.5us	74us	74.5us	Dummy CLK1-10 Keep 1 CLK Period	

Notes:

1. 1H=7.4us.
2. CLK2~CLK10 High Width is T4, same as CLK1.
3. CLK2~CLK10 Low Width is T5, same as CLK1.
4. CLK2 falling to CLK3 falling, CLK3 falling to CLK4 falling, CLK4 falling to CLK5 falling, CLK5 falling to CL K6 falling, CLK6 falling to CLK7 falling, CLK7 falling to CLK8 falling, CLK8 falling to CLK9 falling, CLK9 fa lling to CLK10 falling, are all T6.
5. When power on, STV0/1 and CLK1~CLK10 should keep low before the first STV0/1.
6. VDDODD and VDDEVEN must reverse in vertical blanking time.
7. Charging sharing function should be set up to by frame.
8. CLK1-10 Keep Dummy CLK 1 CLK Period.
9. VDDODD/VDDEVEN Keep Half Period VGH and Half Period VGL in 1 Period.

6.3 Signal Timing Waveform

H total :4240
V total :2250
Frame Rate:144Hz



6.3 Signal Timing Waveform

H total :4240
V total :2250
Frame Rate:144Hz

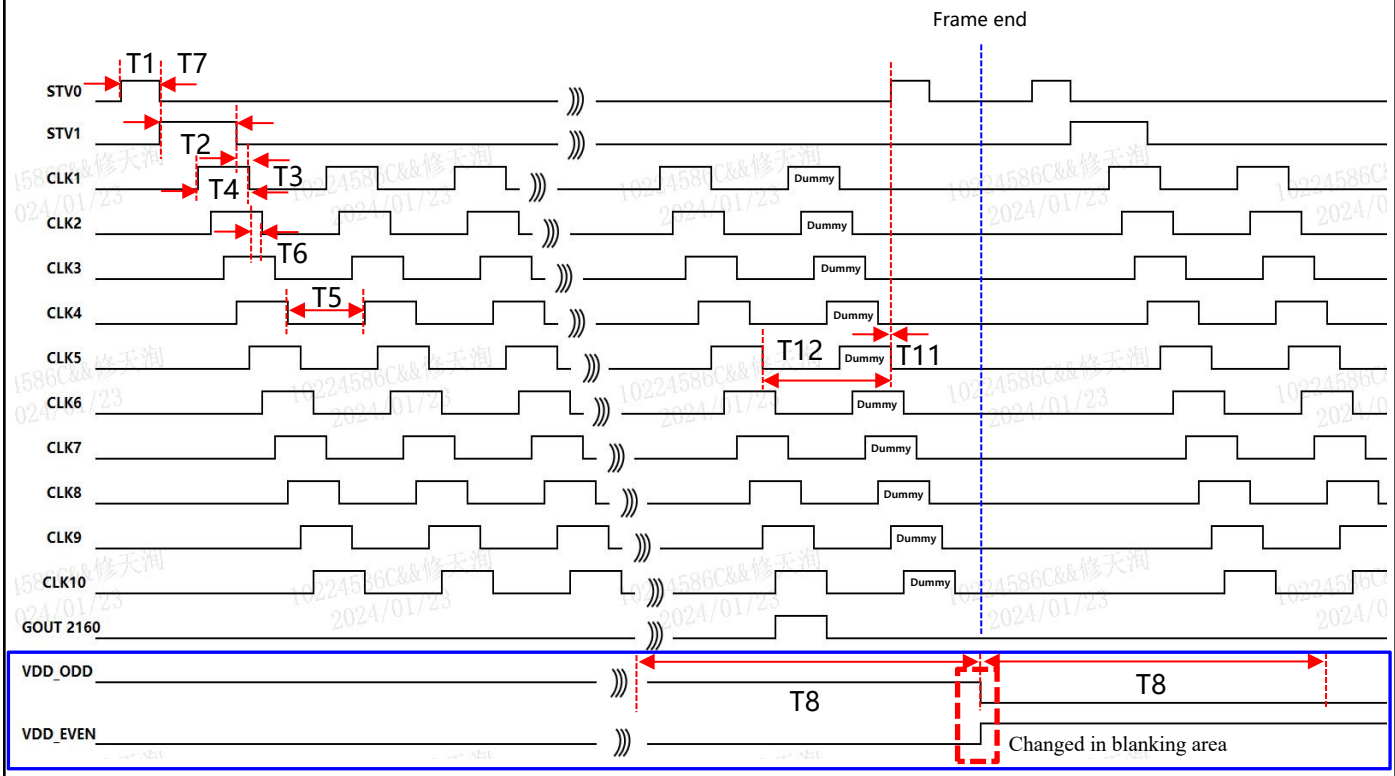
	Min.	Typ.	Max.	Description	Remark
T1	18.41us	18.51us	18.61us	STV0 Width(3H)	
T2	36.92us	37.02us	37.12us	STV1 Width(6H)	
T3	6.12us	6.17us	6.22us	STV1 Falling to CLK Falling(1H)	
T4	24.58us	24.68us	24.78us	CLK High Width(4H)	
T5	36.92us	37.02us	37.12us	CLK Low Width(6H)	
T6	6.12us	6.17us	6.22us	CLK1 Falling to CLK2 Falling(1H)	
T7	0	0	0	STV0 Falling to STV1 Rising	
T8	-	2s	3s	VDDODD/EVEN Changing Period (1 Period of High or Low)	Changed in blanking area
T9	2.9	3.0	3.05	GOE	
T10	-	Refer to CE DS CMD	-	SOE Width	
T11	0	0	6.17us	Dummy CLK5 Falling to STV0 Rising	
T12	61.6us	61.7us	61.8us	Dummy CLK1-10 Keep 1 CLK Period	

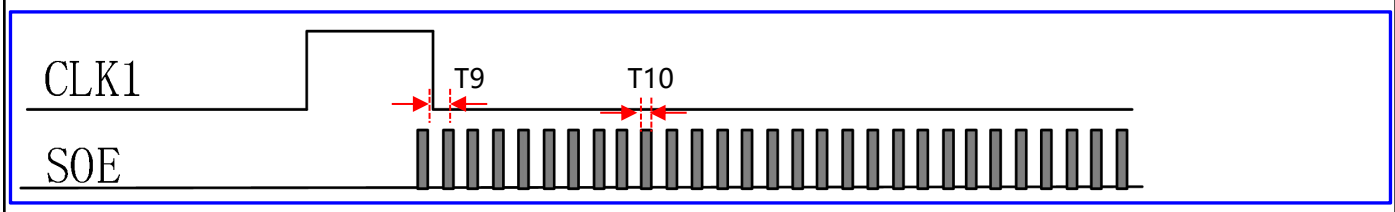
Notes:

1. 1H=6.17us.
2. CLK2~CLK10 High Width is T4, same as CLK1.
3. CLK2~CLK10 Low Width is T5, same as CLK1.
4. CLK2 falling to CLK3 falling, CLK3 falling to CLK4 falling, CLK4 falling to CLK5 falling, CLK5 falling to CL K6 falling, CLK6 falling to CLK7 falling, CLK7 falling to CLK8 falling, CLK8 falling to CLK9 falling, CLK9 fa lling to CLK10 falling, are all T6.
5. When power on, STV0/1 and CLK1~CLK10 should keep low before the first STV0/1.
6. VDDODD and VDDEVEN must reverse in vertical blanking time.
7. Charging sharing function should be set up to by frame.
8. CLK1-10 Keep Dummy CLK 1 CLK Period.
9. VDDODD/VDDEVEN Keep Half Period VGH and Half Period VGL in 1 Period.

6.3 Signal Timing Waveform

H total :4240
V total :2250
Frame Rate:165Hz





6.3 Signal Timing Waveform

H total :4240
V total :2250
Frame Rate:165Hz

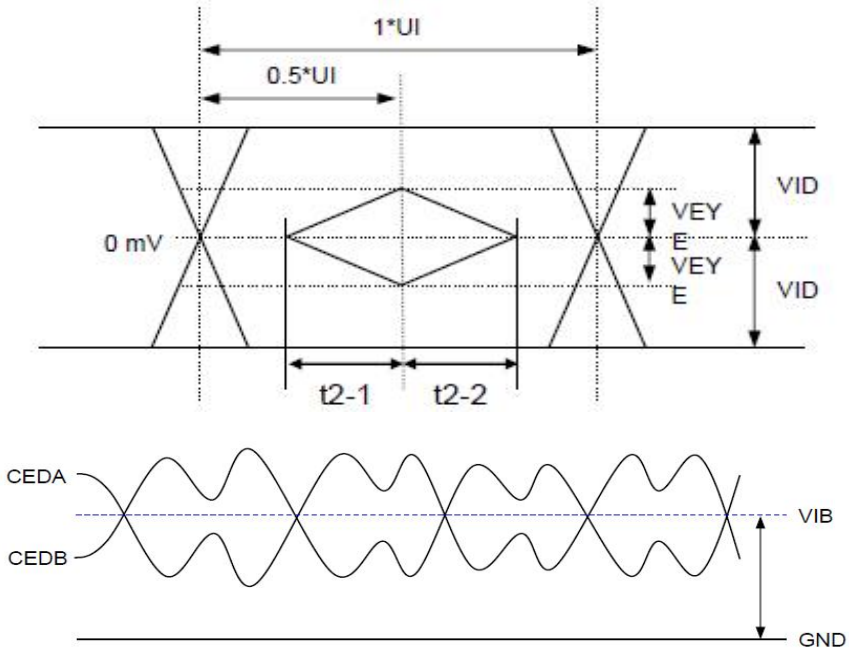
	Min.	Typ.	Max.	Description	Remark
T1	16.07us	16.17us	16.27us	STV0 Width(3H)	
T2	32.24us	32.34us	32.44us	STV1 Width(6H)	
T3	5.34us	5.39us	5.44us	STV1 Falling to CLK Falling(1H)	
T4	21.46us	21.56us	21.66us	CLK High Width(4H)	
T5	32.24us	32.34us	32.44us	CLK Low Width(6H)	
T6	5.34us	5.39us	5.44us	CLK1 Falling to CLK2 Falling(1H)	
T7	0	0	0	STV0 Falling to STV1 Rising	
T8	-	2s	3s	VDDODD/EVEN Changing Period (1 Period of High or Low)	Changed in blanking area
T9	2.9	3.0	3.05	GOE	
T10	-	Refer to CE DS CMD	-	SOE Width	
T11	0	0	5.39us	Dummy CLK5 Falling to STV0 Rising	
T12	53.8us	53.9us	54us	Dummy CLK1-10 Keep 1 CLK Period	

Notes:

1. 1H=5.39us.
2. CLK2~CLK10 High Width is T4, same as CLK1.
3. CLK2~CLK10 Low Width is T5, same as CLK1.
4. CLK2 falling to CLK3 falling, CLK3 falling to CLK4 falling, CLK4 falling to CLK5 falling, CLK5 falling to CL K6 falling, CLK6 falling to CLK7 falling, CLK7 falling to CLK8 falling, CLK8 falling to CLK9 falling, CLK9 fa lling to CLK10 falling, are all T6.
5. When power on, STV0/1 and CLK1~CLK10 should keep low before the first STV0/1.
6. VDDODD and VDDEVEN must reverse in vertical blanking time.
7. Charging sharing function should be set up to by frame.
8. CLK1-10 Keep Dummy CLK 1 CLK Period.
9. VDDODD/VDDEVEN Keep Half Period VGH and Half Period VGL in 1 Period.

6.4 Signal Eye Diagram

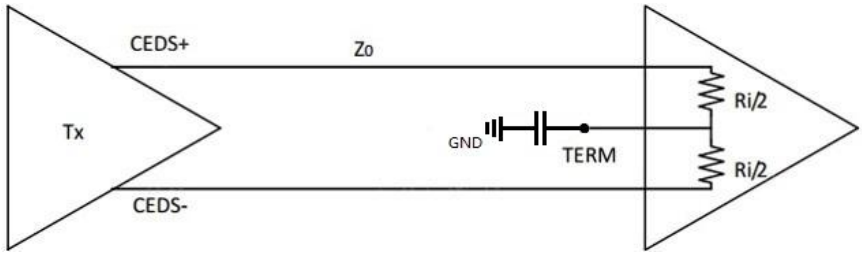
< Table 13. CEDS Eye Diagram >



Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Veye	VEYE	75	-	250	mV	
Eye-Open time	t2-1, t2-2	0.25	-	-	UI	
CEDS Bandwidth	FCEDS	1.2	-	3.15	Gbps	
CEDS input differenctial voltage	VID	150	-	500	mV	
CEDS input common voltage	VIB	0.65	(DVDD1V8S & DVDD1V9S)/2	(DVDD1V8S & DVDD1V9S-0.6)-VID/2	V	For LVDS Application

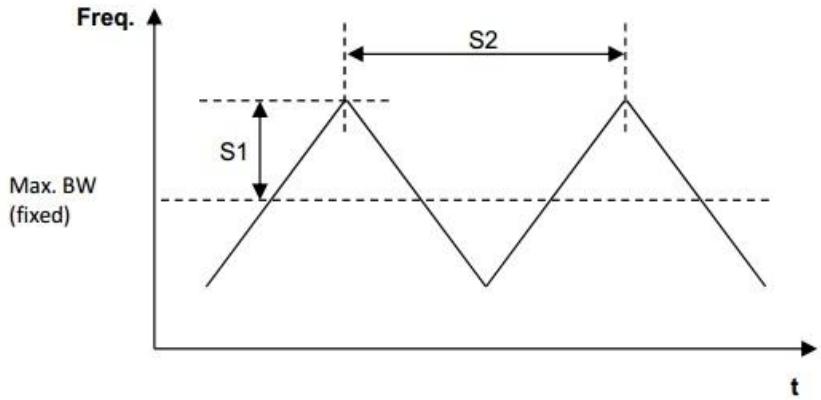
Notes :
1. Eye diagram test point is located on source board, close to source driver.
2. UI: Unit Interval.
3. This product use LVDS type of CEDS input common voltage only.

6.4 Signal Eye Diagram



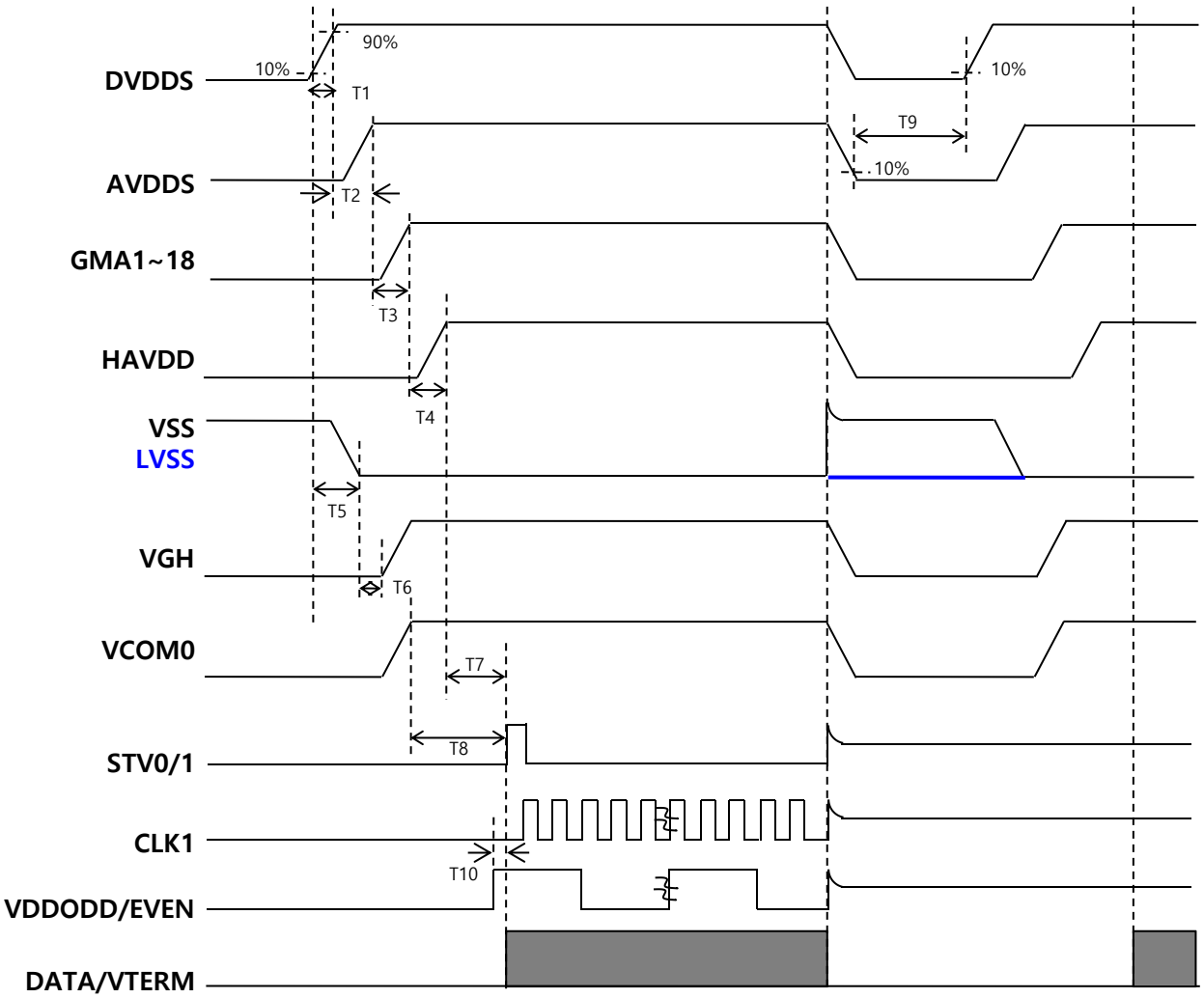
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Transmission Line impedance	Z0	-	50	-	Ω	CEDS Tx to CEDS Rx
Input termination resistance	Ri	90	100	110	Ω	CEDS0A to CEDS0B

< Table 14. CEDS SSC Modulation >



Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Modulation Ratio of SSC	S1	-1	-	+1	%	Modulation Freq.=100kHz
		-2	-	+2	%	Modulation Freq.=Under 50kHz
Modulation Frequency of SSC	S2	-	-	100	KHz	Modulation Rate=1%

7.0 POWER SEQUENCE



Notes :

1. When power off, VGL(VSS),STV,CLK,VDDODD/VDDEVEN timing should follow VGH falling.
2. VGH is on SOC board or separate power board only, so T6 time is tested on SOC board or separate power board.
3. VDDODD/VDDEVEN must keep reverse phase after 1st STV0 rising edge when power on.

7.0 POWER SEQUENCE

T	Min	Type	Max	Unit	Note
T1	0	-	10	ms	
T2	0	-	-	ms	
T3	0	-	-	ms	AVDDS must be higher than HAVDD and GMA all the time
T4	-T3	-	1000	ms	AVDDS must be higher than HAVDD and GMA all the time
T5	0	-	-	ms	
T6	0	-	-	ms	
T7	0	-	-	ms	
T8	0	-	-	ms	
T9	1	-	-	s	
T10	50	-	-	ms	VDD should pull high before 1st STV rising

8.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

< Table 15. Reliability Test Parameters >

No	Test Items	Conditions
1	High temperature storage test	Ta = 60 ℃, 240 hrs
2	Low temperature storage test	Ta = -20 ℃, 240 hrs
3	High temperature & high humidity operation test	Ta = 50 ℃, 80%RH, 240hrs
4	High temperature operation test	Ta = 50 ℃, 240hrs
5	Low temperature operation test	Ta = -5 ℃, 240hrs
6	Thermal shock	Ta = -20 ℃ ↔ 60 ℃ (0.5 hr), 100 cycle

Note : Test condition is based on BOE module.

9.0 PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD Open Cell.

9.1 Precautions when taking out the Panel

- Pick the pouch only, when taking out panel from a shipping package.
- Recommend to use suitable sucker to pick up and put down panel.

9.2 Precautions for handling the panel

- As the electrostatic discharges may break the LCD panel, handle the LCD panel with care. Peel a protection sheet off from the LCD panel surface as slowly as possible. Refer to the appendix 3.
- As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD panel should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Put the panel display side down on a flat horizontal plane.
- Handle connectors and cables with care.

9.3 Precautions for the operation

- The LCD product shall be operated under normal conditions as below:
  - Temperature: 20±15℃
  - Humidity: 55±20%
  - Display pattern: continually changing pattern(Not stationary)
- Product reliability and functions are only guaranteed when the product is used under right operation usages. If product will be used in extreme conditions such as high temperature, high humidity, high altitude, special display patterns, long time operation, outdoor operation, etc.., it is strongly recommended to contact BOE for the advice about the application of engineering. Otherwise its reliability and function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock markets, and controlling systems.
- Do not exceed the absolute maximum rating value.
- Periodical power-off or screen save is needed after long-term display. Product reliability and functions may not be guaranteed when it under 24 hours operation continuously per day.

9.0 PRECAUTIONS

- Do not insert or pull out the interface connector while the LCD panel is operating.
- LCD Response time depends on the temperature.(In lower temperature, it becomes longer)
- Ensure all input signals and power supplies are complete and valid when the panel is operating. Otherwise the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the panel would be damaged. Specially, pay attention to the turn on and off sequence.

9.4 Precautions for the atmosphere

- Recommend storage atmosphere

ITEM	UNIT	MIN	MAX
Storage Temperature	(℃)	5	40
Storage Humidity	(%RH)	35	75
Storage Life	6 months		
Storage Condition	• The storage room should be equipped with a dark and good ventilation facility. • Prevent products from being exposed to the direct sunlight, moisture and water. • The product need to keep away from organic solvent and corrosive gas. • Be careful for condensation at sudden temperature change. • Storage condition is guaranteed under packing conditions.		

- Dew drop atmosphere should be avoided. When expose to drastic fluctuation of temperature (hot to cold or cold to hot), the LCD module may be affected. Specifically, drastic temperature fluctuation from cold to hot, produces dew on the LCD module's surface which may affect the operation of the polarizer and LCD module.
- Do not store and/or operate the LCD panel in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

9.5 Precautions for the panel characteristics

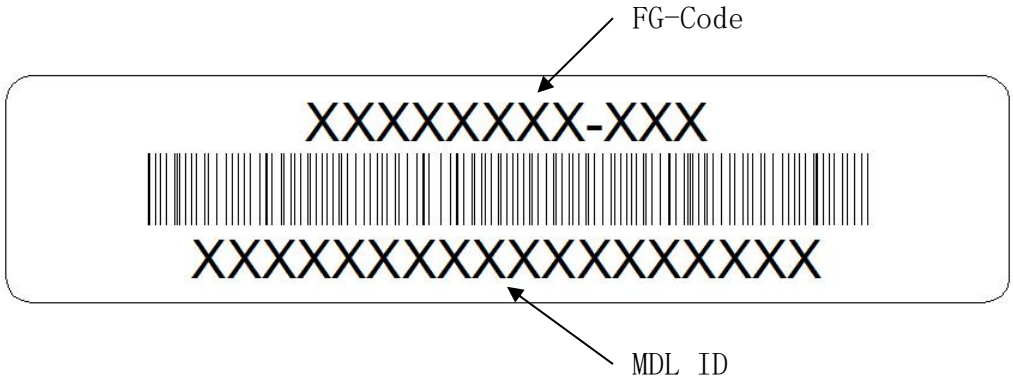
- Do not apply fixed pattern data signal to the LCD panel at product aging.
- Applying fixed or weak signal pattern (low resolution or interlaced scanning video) for a long time may cause image sticking.

9.0 PRECAUTIONS

9.6 Other precautions

- In particular in winter, Before putting Panel boxes on the line, aging process is required to make the temperature of products similar to the temperature of workplace.
- Do not disassemble and/or re-assemble LCD panel.
- Do not re-adjust variable resistor or switch etc.
- When returning the panel for repair or etc., Please pack the panel not to be broken. We recommend to use the original shipping packages.
- Product assembled into module should be stored in the bag(cover case).
- Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- Be careful not to give any extra mechanical stress to the panel when designing the set, and backlight.
- Do not pull, fold or bend the source COF and the gate COF in any processes.
- If the liquid crystal material leaks from the panel, this should be kept away from the eyes or mouth. If this contacts to hands, legs, or clothes, you must washed it away with soap thoroughly and see a doctor for the medical examination.

10.0 PRODUCT SERIAL NUMBER



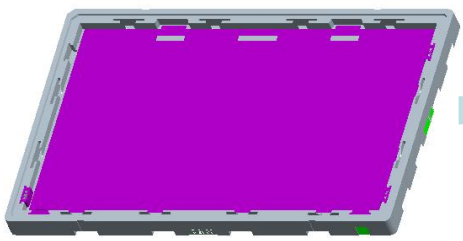
MDL ID Naming Rule:

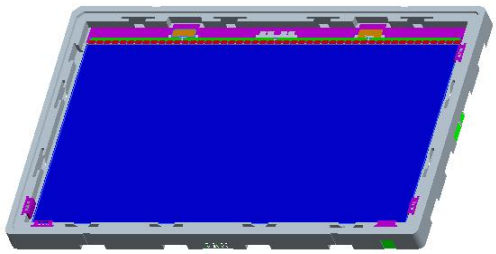
Digit / Code	1	2	3	4	5	6	7	8	9	10	11
Description	Model Code GBN		Grade	Line	Year		Month	Model Extension Code			
Digit / Code	12	13	14	15	16	17	18				
Description	Serial No						扫码不显示，BOE厂内用				

11.0 PACKING INFORMATION

BOE provides the standard shipping container for customers, unless customer specifies their packing information. The standard packing method and Barcode information are shown in the below.

11.1 Packing Order

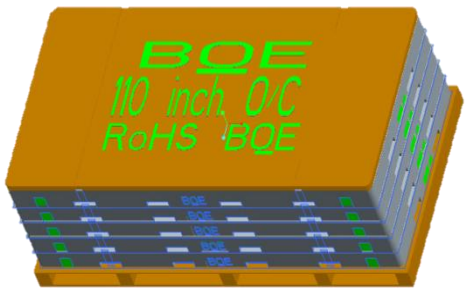


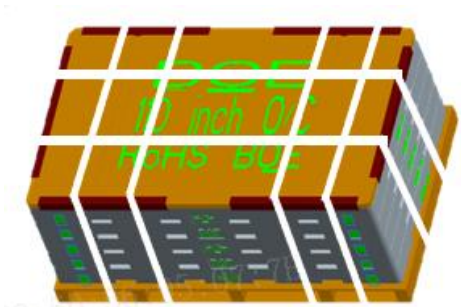


- Put one EPE+AL pad on the Box
- Then put one OC on the Pad，n ext put one anti-slip EPE Pad.

Finger position marks desiccant location.

- In this way, put 7 pcs anti-slip EP E Pad,8 pcs OC……. Finally , put one anti-slip EPE Pad on the top.
- 12 ea Driers in the Box





- Put 5ea EPS Box and 1ea EPS Cover on the Pallet
- Totally: 5ea Box.1ea Cover,40pcs OC,60ea Driers in one Pallet

- Place Paper Corner and wrap film around the boxes.
- Pack with 6 packing belts.

Cautions：

When transferring in warehouse or factory, the arm length of electric forklift or hand pall et truck must be longer than the pallet along the insertion direction.

11.2 Packing Note

- Box Dimension : 2715mm(L)×1746mm(W)×160mm(H)
- Package Quantity in one Box : 8 pcs

11.3 Box Label

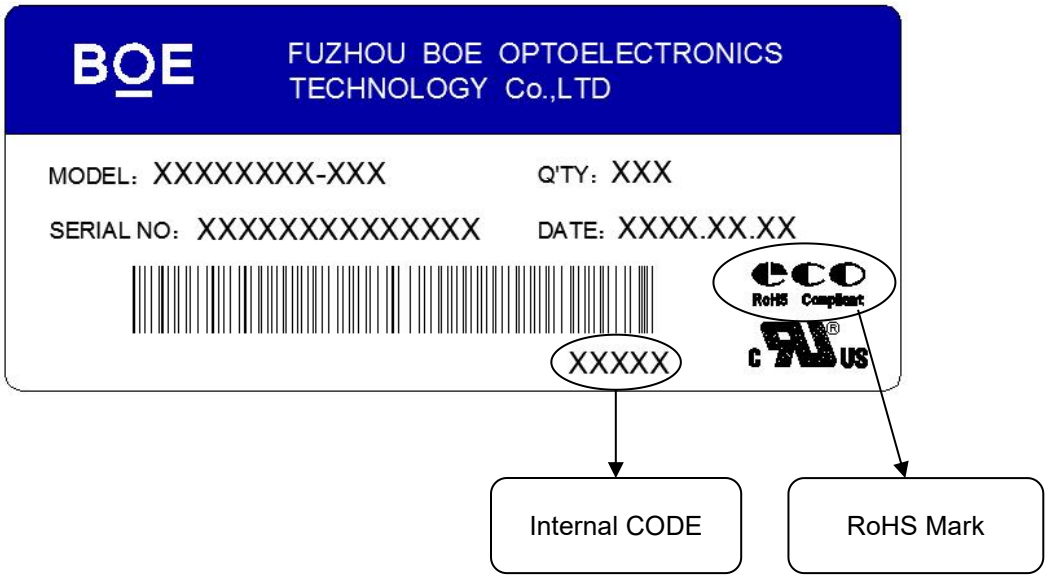
- Label Size : 70 mm (L) × 30 mm (W)
  - Contents

    Model : HV110QUB-E10

    Q`ty : OC  8 Q`ty in one box

    Serial No. : Box Serial No.

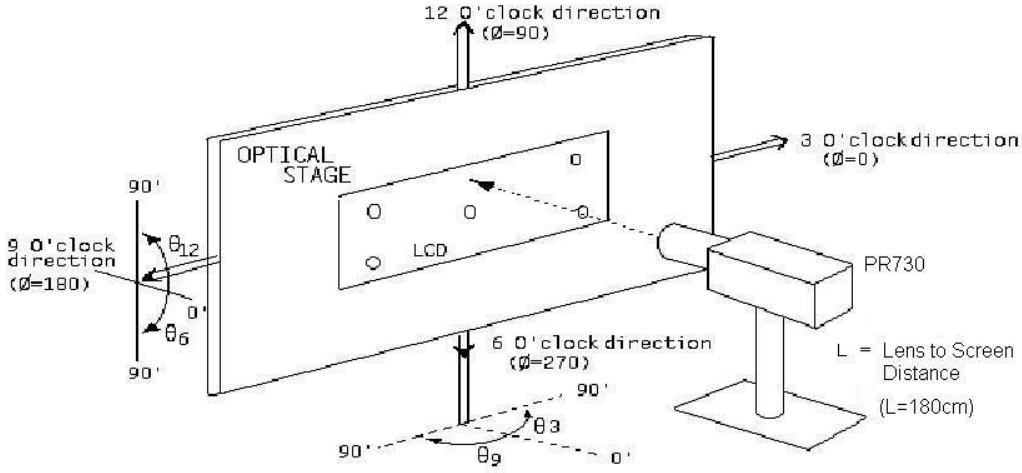
    Date : Packing Date



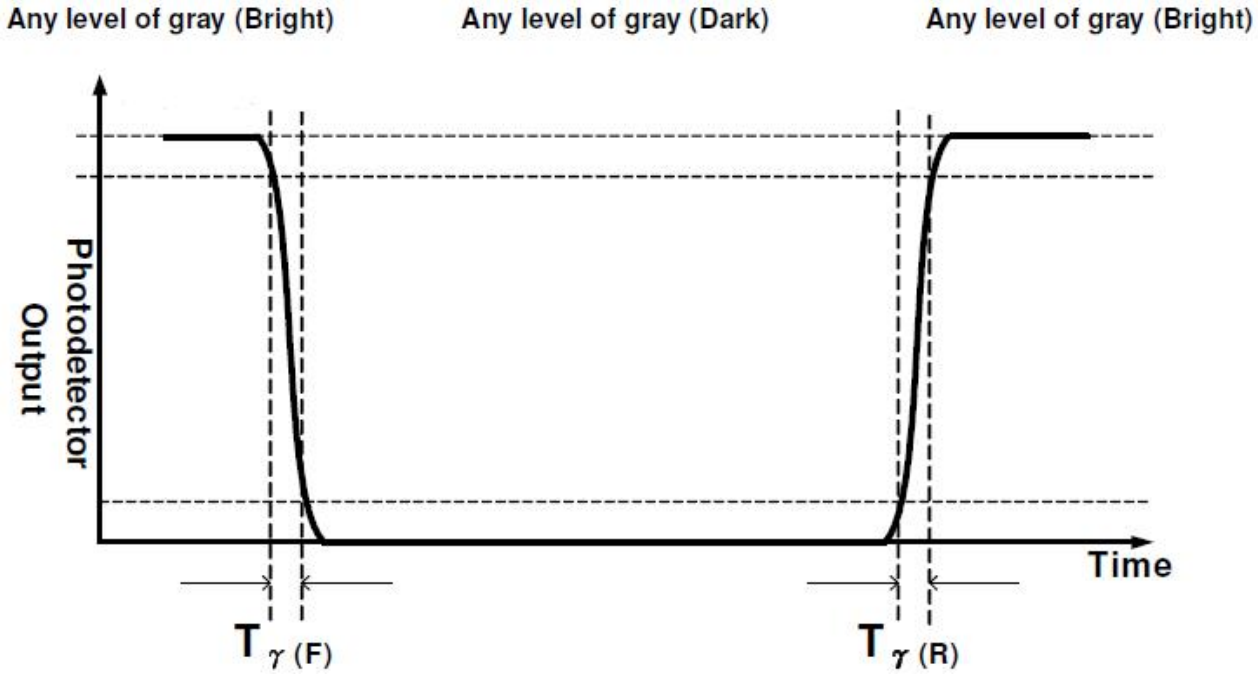
Box ID Naming Rule:

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Description	Products GBN		Grade	Line	Year		Month	Revision Code	Serial No				

12.0 APPENDIX 1

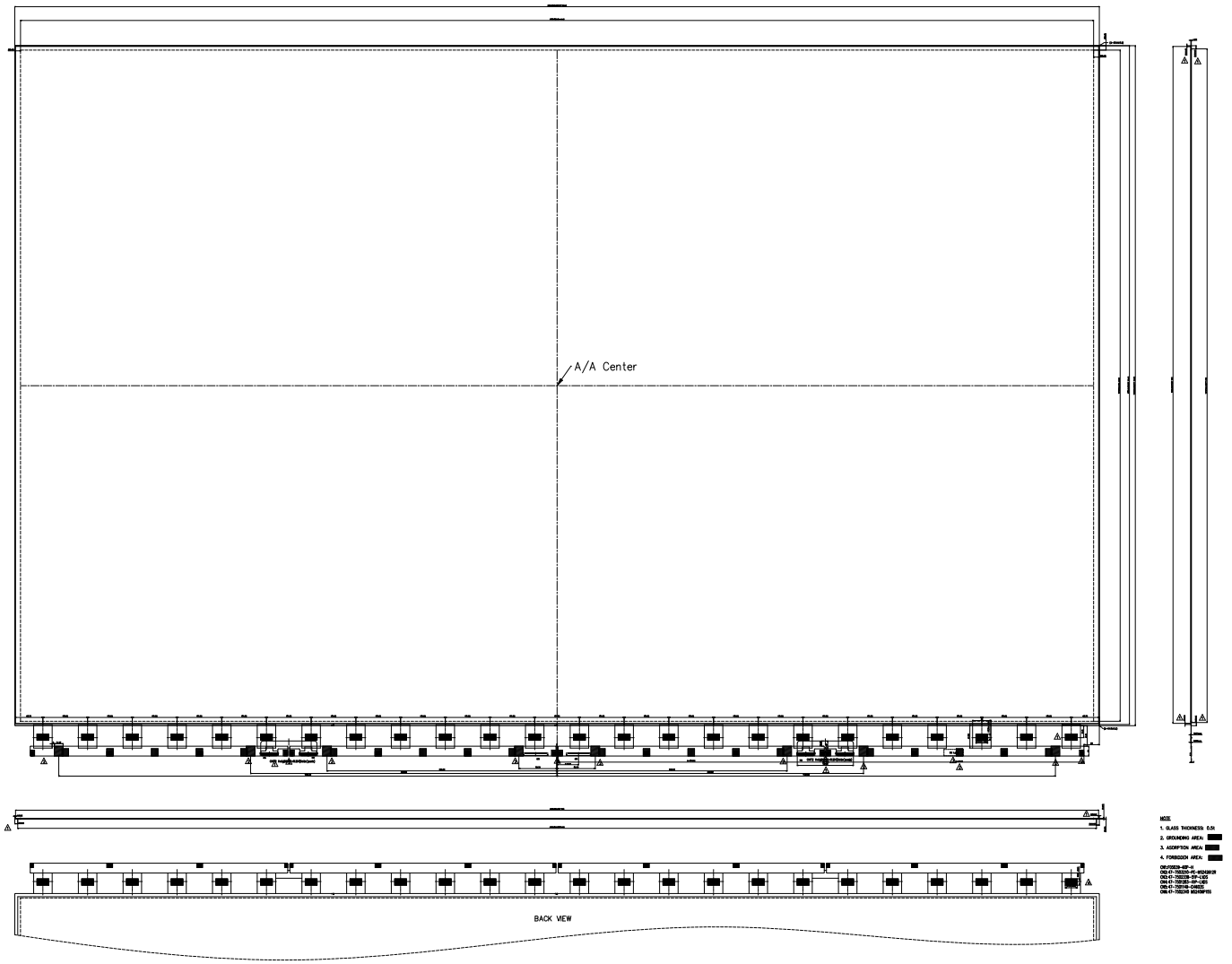


< Figure 1. Measurement Set Up >



< Figure 2. Response Time Testing >

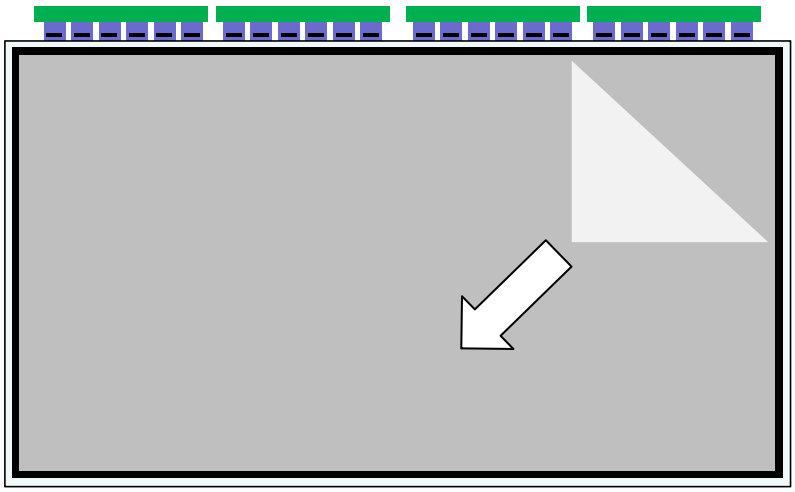
12.0 APPENDIX 2



< Figure 3. TFT-LCD Open Cell Outline Dimensions (Front View) >

Tolerance Ta ble(±)				
Dimension	1 Grade	2 Grade	3 Grade	4 Grade
L ≤20	0.05	0.1	0.1	0.2
20 < L ≤50	0.1	0.15	0.2	0.25
50 < L ≤100	0.15	0.2	0.25	0.3
100 < L ≤200	0.2	0.25	0.3	0.5
200 < L	0.25	0.3	0.5	0.8
Unless Otherwise Specified				

12.0 APPENDIX 3



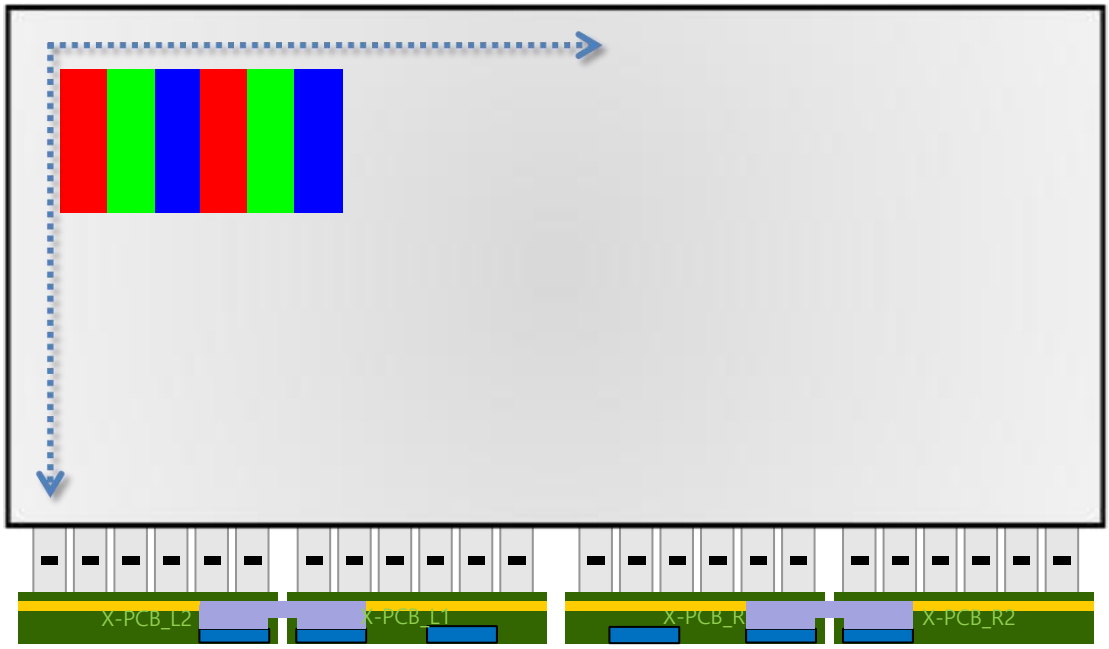
< Figure 4. TFT POL Protect Film Peeling Method >

Peeling Step:

1. Be sure to peel off slowly(recommended more than 7sec) and constant speed.
2. Peeling direction shows in Figure 4.
3. Be sure to ground person with adequate methods such as the anti-static wrist band.
4. Be sure to ground each source PCB while peeling off the protection film.
5. Ionized air should be blown over during peeling action.
6. The protection film must not touch drivers and source PCBs.
7. If adhesive may remain on the polarizer after the protection film peeling off, please remove with isopropyl-alcohol.

12.0 APPENDIX 4

This product is reverse type display. RGB data mapping scan direction : from left-up to right-down.



< Figure 5. Display Mode>