TITLE : HV650QUB-F9L

Product Specification

Rev.O

Hefei BOE Display Technology Co., Ltd.

REVISION HISTORY

( ) Preliminary specification
(√) Final specification

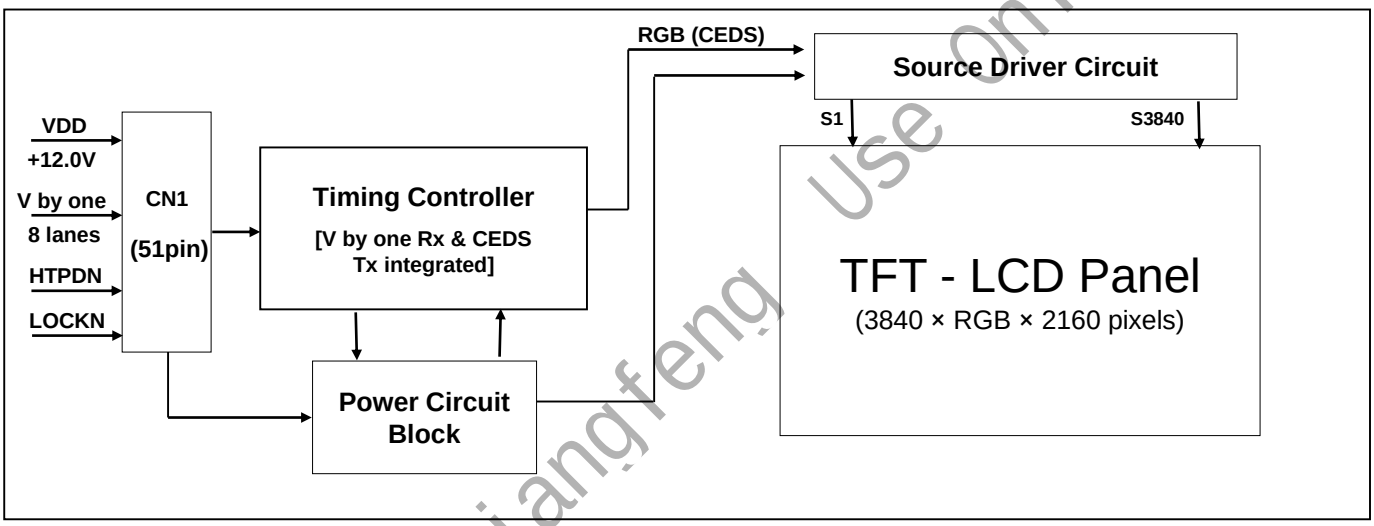
	Page	Description of changes	Date	Prepared
O	All	Initial Release	2022.09.27	Chen Hangyu

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

HV650QUB-F9L is a color active matrix TFT LCD open cell using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 64.5 inch diagonally measured active area with UHD resolutions (3840 horizontal by 2160 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in Z-inversion stripe and this module can display 1.07G colors. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.



1.2 Features

- V by one interface with 8 lanes
- High-speed response
- Low color shift image quality
- 8-bit + FRC color depth, display 1.07G colors
- High luminance and contrast ratio, low reflection and wide viewing angle
- Gate driver use GOA mode
- DE (Data Enable) only mode
- ADS technology is applied for high display quality
- RoHS compliant
- We didn't use substances and uses prohibited in 《SS-00259 for general use》

1.3 Application

- Home Alone Multimedia TFT-LCD TV only
- Ultra High Definition TV(UHD TV)
- Display Terminals for Control System, Public Monitor and etc… are not allowed

1.4 General Specification

< Table 1. General Specifications >

Parameter	Specification	Unit	Remark
OC Size	1440.48(H) × 817.02(V) × 1.32(D)	mm	H&V±0.2/D±0.1
Active area	1428.48(H) × 803.52(V)	mm	
Number of pixels	3840(H) ×2160(V)	pixels	
Pixel pitch	372(H) ×372(V)	㎛	
Pixel arrangement	Pixels RGB Z-inversion stripe	-	
Display colors	1.07G (8bits + FRC)	colors	
Display mode	Transmission mode, Normally Black		
Open Cell Transmittance	5.1%(TYP.)	%	At center point with BOE BLU
Weight	3500	gram	
Power Consumption	9.86	Watt	With TCON board
Surface Treatment	Front Polarizer：Haze 1%, 3H, Semi-glare or Anti-glare treatment Bottom Polarizer：Clear	-	
Protection Film Peeling Force	20(Max)	gf/25mm	Measured by JIS Z 0327

2.0 ABSOLUTE MAXIMUM RATINGS

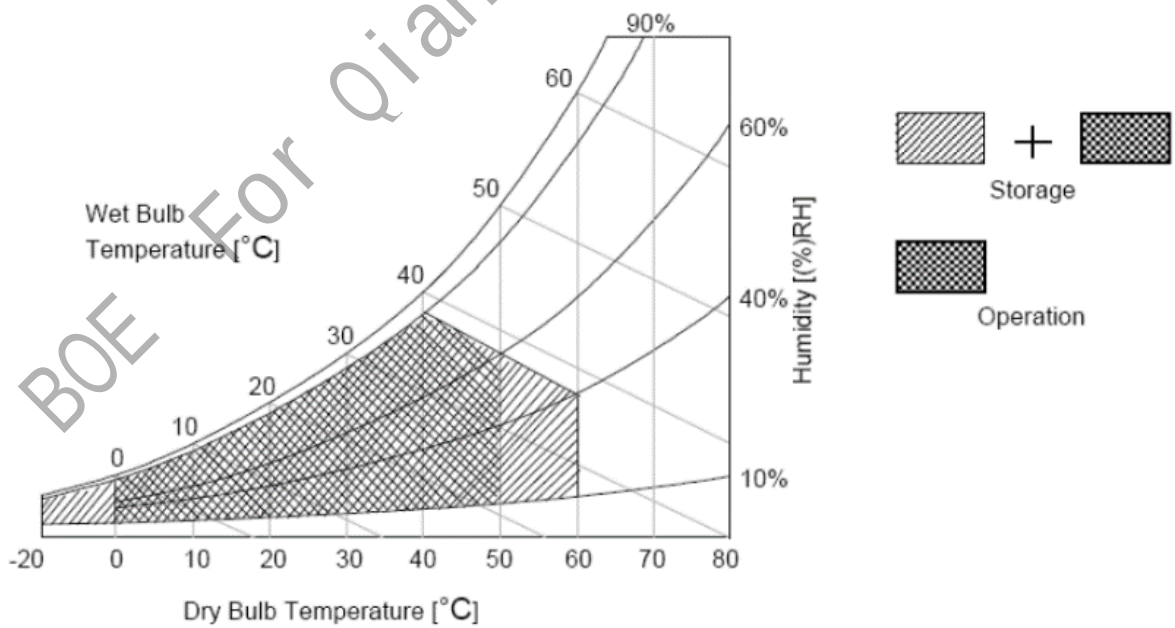
The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum values are listed in the below table.

< Table 2. Open Cell Absolute Maximum Ratings >

[VSS=GND=0V]

Parameter	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD	VSS-0.3	+13.5	V	Ta=25℃
CMOS/TTL Input Voltage	DVDD	VSS-0.3	+3.6	V	
Operating Temperature	T_{OP}	0	+50	℃	Note 1
	T_{SUR}	0	+65	℃	
Storage Temperature	T_{ST}	-20	+60	℃	
Operating Ambient Humidity	Hop	10	90	%RH	
Storage Humidity	Hst	5	90	%RH	

Note 1: Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 ℃ max. and no condensation of water.



3.0 ELECTRICAL SPECIFICATIONS

3.1 TFT LCD Open Cell

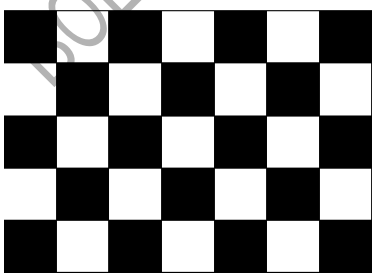
< Table 3. Open Cell Electrical Specifications >

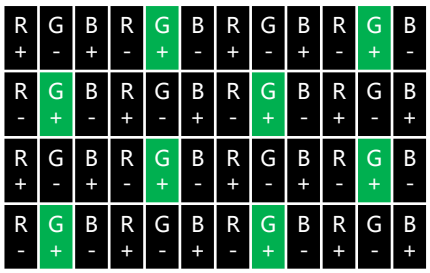
[Ta =25±2 ℃]

Parameter		Symbol	Values			Unit	Remark
			Min	Typ	Max		
Power Supply Input Voltage		VDD	10.8	12	13.2	V	
Power Supply Ripple Voltage		VRP	-	-	600	mV	
Power Supply Current		IDD	-	0.83	2.58	A	Note 1
Power Consumption		PDD	-	9.86	31	Watt	
Rush current		IRUSH	-	-	10	A	Note 2
V by One Interface	Differential Input High Threshold Voltage	VLVTH	-	-	+50	mV	
	Differential Input Low Threshold Voltage	VLVTL	-50	-	-	mV	
	Common Input Voltage	VLVC	-	-	-	V	
	Terminating Resistor	Rt	90	100	110	ohm	
CEDS Interface	Transmission Line Impedance	Z0	-	50	-	ohm	
	Input termination Resistance	Ri	90	100	110	ohm	
CMOS Interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.6	V	

Note 1: The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for VDD=12.0V.
Frame rate f_V= 60Hz and Clock frequency = 74.25MHz.
Test Pattern of power supply current.

a) Typ : Mosaic 7X5 (L0/L255) b) Max : Horizontal 1 Line (L0/L255) c) Flicker Test Pattern





2: The duration of rush current is about 2ms and rising time of power input is 1ms(min)

3.2 Temperature Characteristics

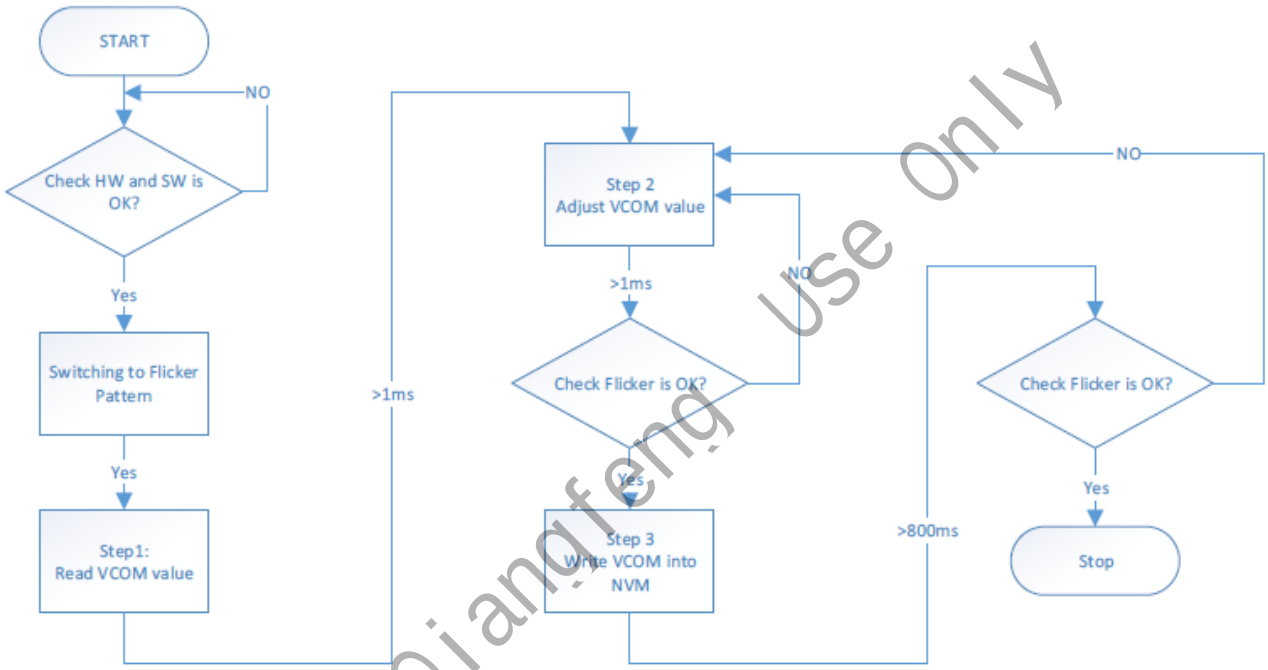
< Table 4. Temperature Characteristics >

Parameter	Symbol	Values			Unit	Remark
		Min	Typ	Max		
Driver Surface Temperature	T_{DS}	-	-	125	℃	Note1
TCON Surface Temperature	T_{TS}	-	-	100	℃	Note2
PMIC Surface Temperature	T_{PS}	-	-	100	℃	Note3

Note 1. Any point on the driver surface must be less than 125 ℃ under any conditions.
2. Any point on the TCON surface must be less than 100 ℃ under any conditions.
3. Any point on the PMIC surface must be less than 100 ℃ under any conditions.
4. This test condition is based on BOE module.

3.3 VCOM I2C Bus Format and interval setting requirement

1. **Initialize (Hardware/Software) Setting and correctly communicate with each other.**
2. **Adjust PVCOM Flow Chart**



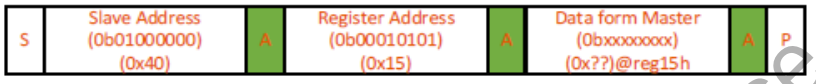
Note 1:

Register Name	Address in Hex	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VCOM	15		VCOM[6:0]						

3.3 VCOM I2C Bus Format and interval setting requirement

3. Step1: Read VCOM

4. Step 2 Adjust VCOM Value



5. Step 3 Write VOCM Value into NVM

Note 2:

S: start

P: stop

A: ack form slave(iML8970)

A: ack form master

NA: noack

sr: repeated start

4.0 INTERFACE CONNECTION

4.1 V-by-One input connector pin configuration

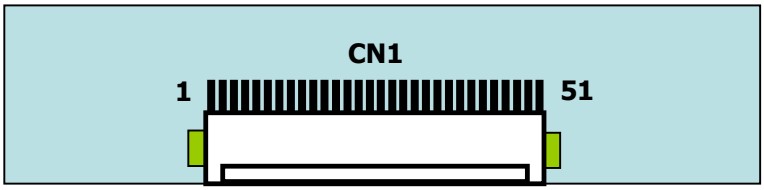
- 51pin Connector: 05030WR-H51B(NC)

< Table 5. 51-Pin V-by-One Input Connector CN1 Pin Configuration>

Pin No	Symbol	Description	Pin No	Symbol	Description
1	VDD	Power Supply +12.0V	27	GND	Ground
2	VDD	Power Supply +12.0V	28	Rx0n	V-by-One HS Data Lane 0
3	VDD	Power Supply +12.0V	29	Rx0p	V-by-One HS Data Lane 0
4	VDD	Power Supply +12.0V	30	GND	Ground
5	VDD	Power Supply +12.0V	31	Rx1n	V-by-One HS Data Lane 1
6	VDD	Power Supply +12.0V	32	Rx1p	V-by-One HS Data Lane 1
7	VDD	Power Supply +12.0V	33	GND	Ground
8	VDD	Power Supply +12.0V	34	Rx2n	V-by-One HS Data Lane 2
9	NC	No Connection	35	Rx2p	V-by-One HS Data Lane 2
10	GND	Ground	36	GND	Ground
11	GND	Ground	37	Rx3n	V-by-One HS Data Lane 3
12	GND	Ground	38	Rx3p	V-by-One HS Data Lane 3
13	GND	Ground	39	GND	Ground
14	NC	No Connection	40	Rx4n	V-by-One HS Data Lane 4
15	NC	No Connection	41	Rx4p	V-by-One HS Data Lane 4
16	NC	No Connection	42	GND	Ground
17	NC	No Connection	43	Rx5n	V-by-One HS Data Lane 5
18	SDA	Tcon_SDA_IN	44	Rx5p	V-by-One HS Data Lane 5
19	SCL	Tcon_SCL_IN	45	GND	Ground
20	nWP	H: Write Enable L&NC: Write Disable	46	Rx6n	V-by-One HS Data Lane 6
21	NC	No Connection	47	Rx6p	V-by-One HS Data Lane 6
22	NC	No Connection	48	GND	Ground
23	Aging Mode	**Valid VBO input：** L&H&NC: Normal display **Invalid VBO input：** L: Black pattern; H&NC: Aging pattern	49	Rx7n	V-by-One HS Data Lane 7
24	GND	Ground	50	Rx7p	V-by-One HS Data Lane 7
25	HTPDN	Hot_plug_detec	51	GND	Ground
26	LOCKN	Lock_detect			

Notes :

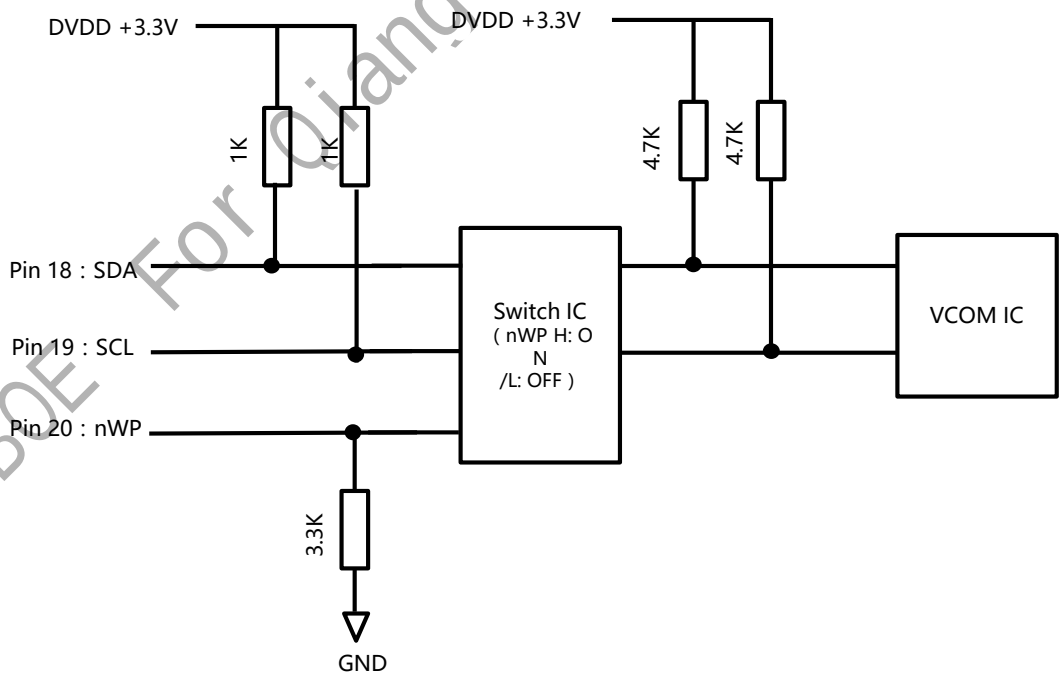
1. NC (Not Connected) : These pins show status of T/con board and are only used for BOE internal operations.
2. Input pins assignments on T/con board refer to the below diagram.



3. If T/con board can't receive correct V-by-One signals, T/con will run BIST pattern as bellow.

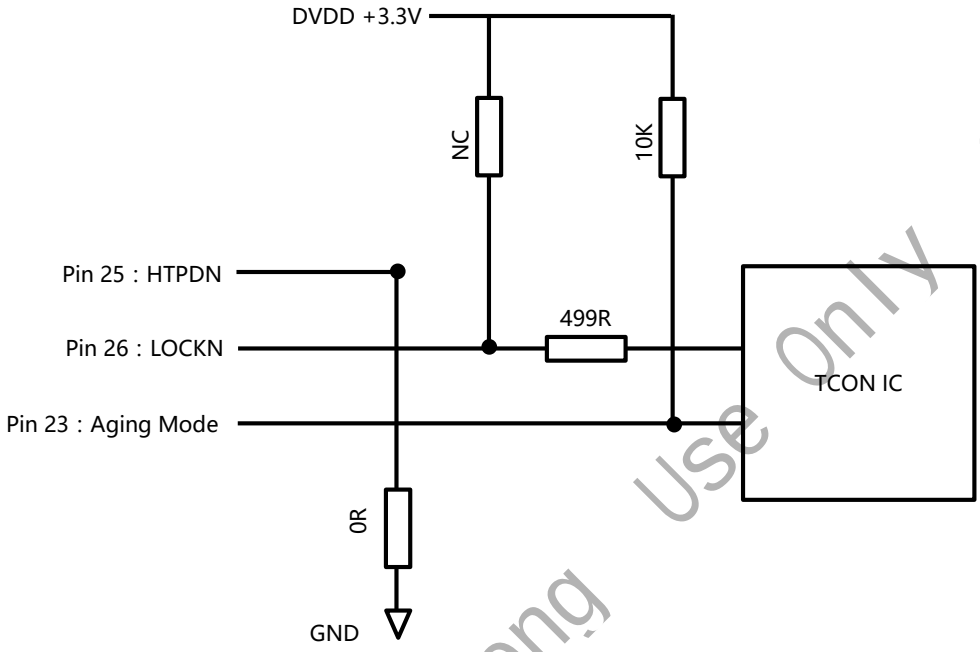
PT1:Black (2 sec)	PT2:White (2 sec)	PT3:Red (2 sec)	PT4:Green (2 sec)	PT5:Blue (2 sec)

4. Circuit Block Diagram pin of SDA/SCL on T/con board. They are used for flicker adjustment only.



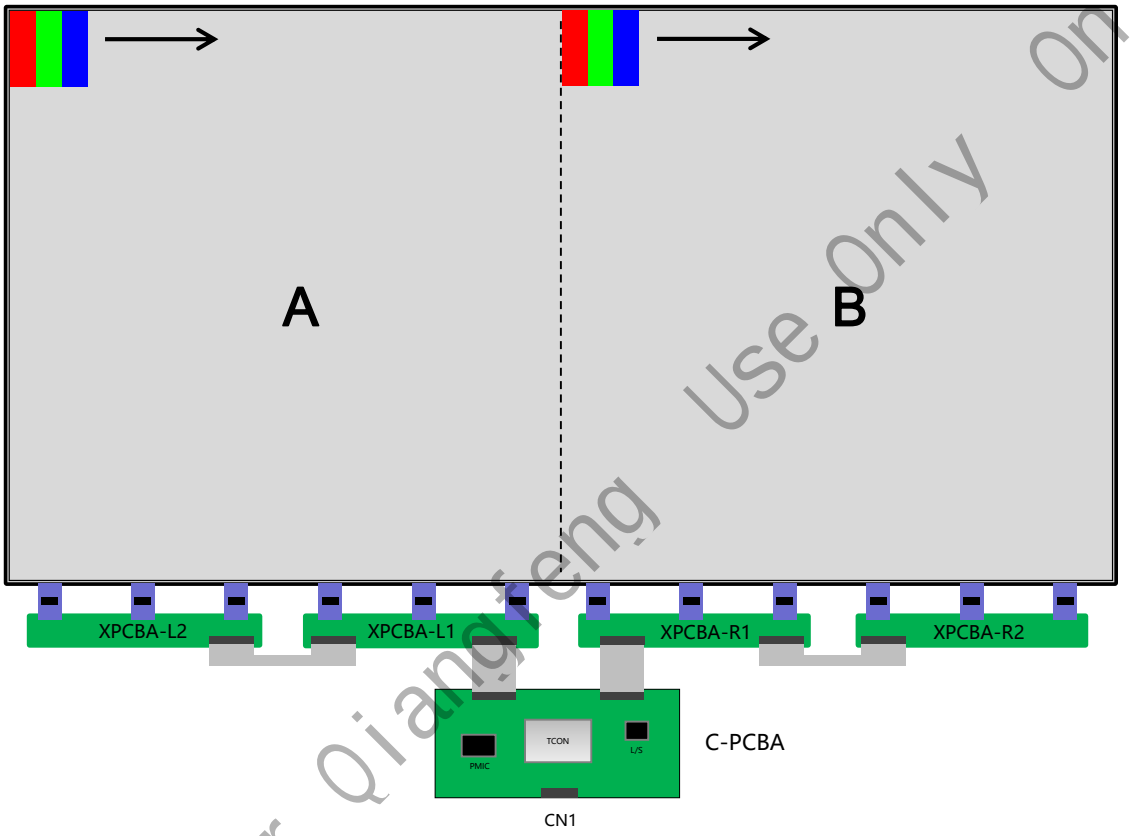
Notes :

5. Circuit Block Diagram of HTPDN/LOCKN/Aging Mode on T/con board.



4.2 V by One Data Mapping Setting

< Table 6. V By One Mapping Diagram >



Connector	V-by-One
CN1	Lane 0 – Lane 7

4.2 V by One Data Mapping Setting

< Table 7. V By One Data Mapping Setting Table >

1 Section					
Area	Lane	Input Data Stream			
		1st	2nd	……	480th
A+B	Lane 0	Pixel 1	Pixel 9	……	Pixel 3833
	Lane 1	Pixel 2	Pixel 10	……	Pixel 3834
	Lane 2	Pixel 3	Pixel 11	……	Pixel 3835
	Lane 3	Pixel 4	Pixel 12	……	Pixel 3836
	Lane 4	Pixel 5	Pixel 13	……	Pixel 3837
	Lane 5	Pixel 6	Pixel 14	……	Pixel 3838
	Lane 6	Pixel 7	Pixel 15	……	Pixel 3839
	Lane 7	Pixel 8	Pixel 16	……	Pixel 3840

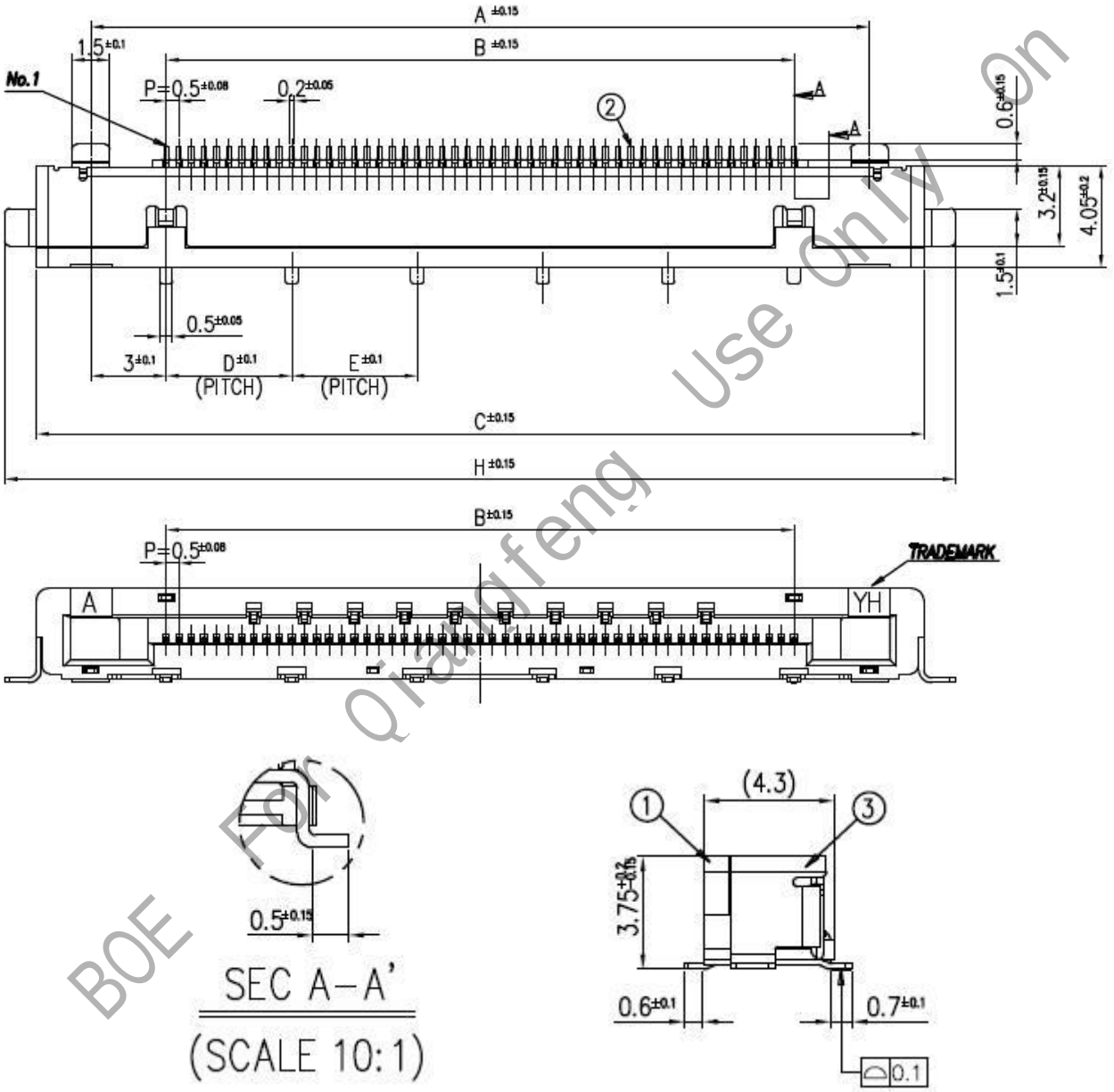
2 Section					
Area	Lane	Input Data Stream			
		1st	2nd	……	480th
A	Lane 0	Pixel 1	Pixel 5	……	Pixel 1917
	Lane 1	Pixel 2	Pixel 6	……	Pixel 1918
	Lane 2	Pixel 3	Pixel 7	……	Pixel 1919
	Lane 3	Pixel 4	Pixel 8	……	Pixel 1920
B	Lane 4	Pixel 1921	Pixel 1925	……	Pixel 3837
	Lane 5	Pixel 1922	Pixel 1926	……	Pixel 3838
	Lane 6	Pixel 1923	Pixel 1927	……	Pixel 3839
	Lane 7	Pixel 1924	Pixel 1928	……	Pixel 3840

Note: T/con board supports two kinds of sections. System board output can choose either of them.

4.0 INTERFACE CONNECTION

4.3 TCON Board Input Connector & FFC Drawing

-51pin Connector Drawing-05030WR-H51B(NC)

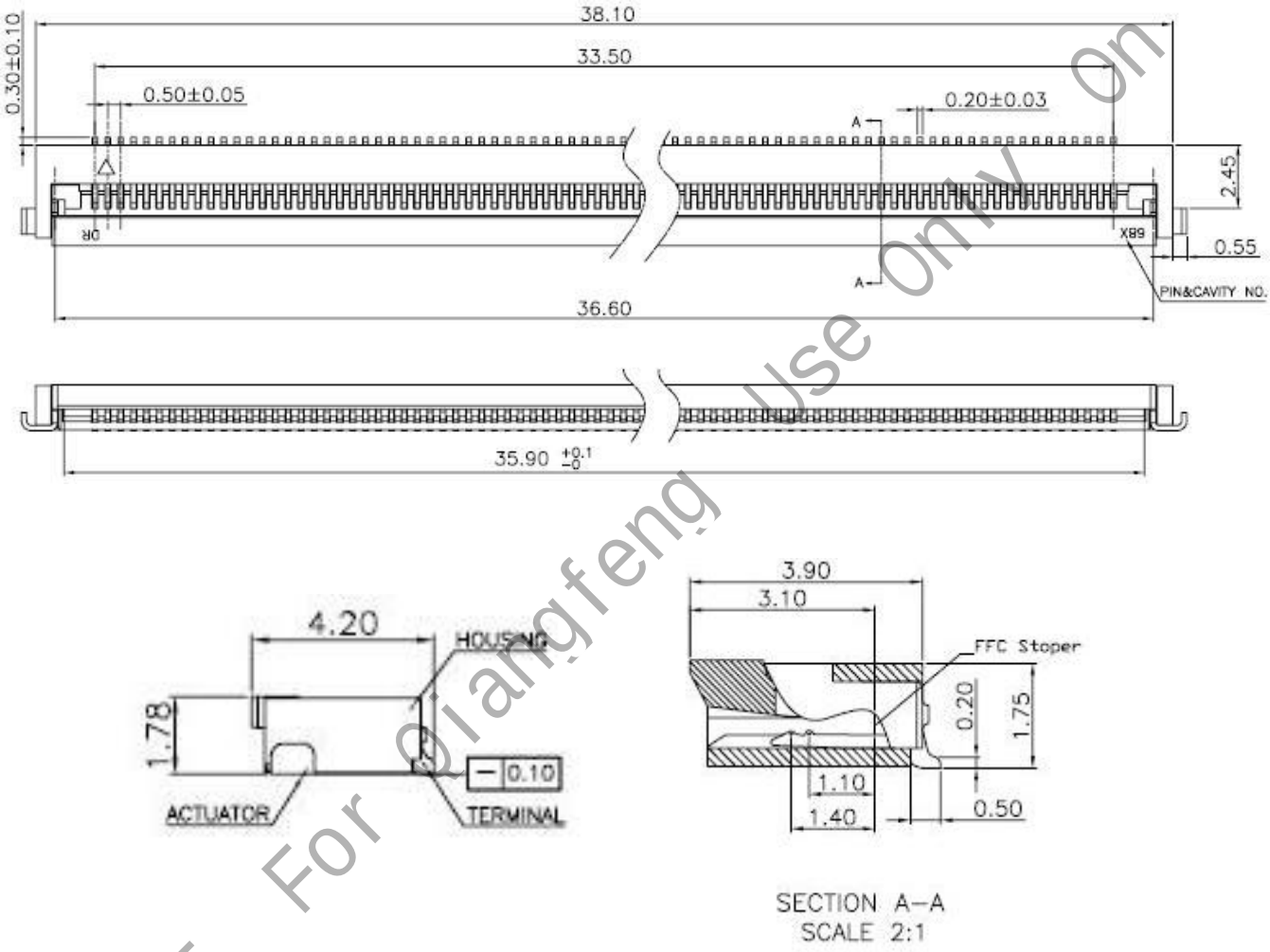


NO. OF POS.	PARTS NO.	A	B	C	D	E	F	G	H
51	05030WR–H51B	31.0	25.0	35.35	5	5	35.95	34.75	38.00

4.0 INTERFACE CONNECTION

4.4 TCON Board Output Connector & FFC Drawing

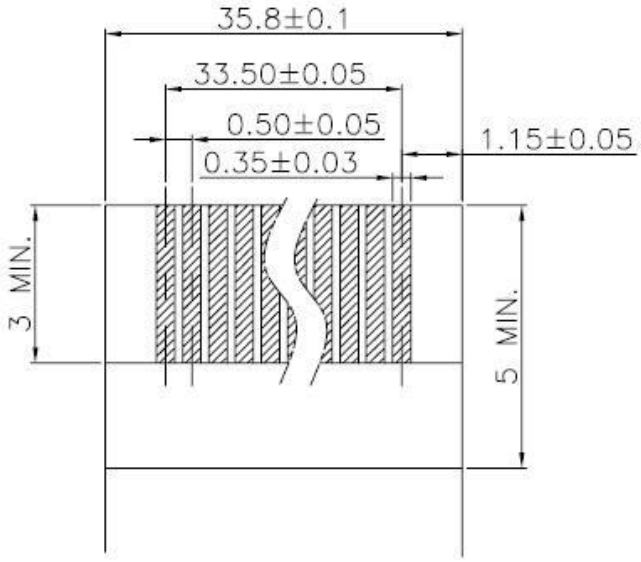
-68pin Connector Drawing-FC0568-L3920W420H180-N03



Note: XPCB board input connector is the same as T/con board output connector.

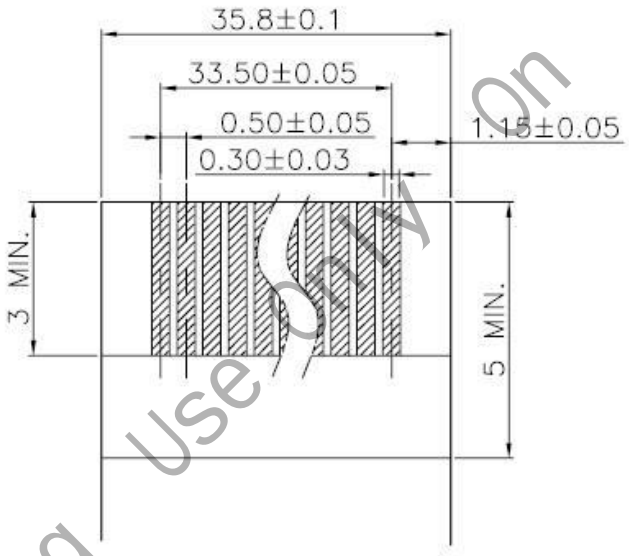
4.4 TCON Board Output Connector & FFC Drawing

-68pin FFC Drawing



RECOMMENDED FFC DIM.

THICKNESS:0.3±0.03



RECOMMENDED FPC/FFC DIM.

THICKNESS:0.3±0.03

Notes: This FFC drawing is supplied by the connector vendor. It is for reference only.

5.0 INTERFACE SIGNAL TIMING SPECIFICATION

5.1 V by One signal specification

- Vx1 Byte length and Color mapping

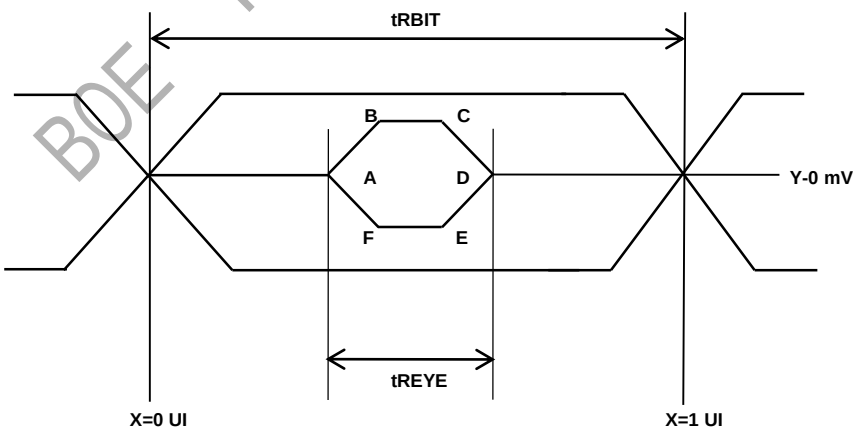
Byte	Packer input	Color data mapping
		30 bpp RGB
0	Bit-0	R2
	Bit-1	R3
	Bit-2	R4
	Bit-3	R5
	Bit-4	R6
	Bit-5	R7
	Bit-6	R8
	Bit-7	R9
1	Bit-8	G2
	Bit-9	G3
	Bit-10	G4
	Bit-11	G5
	Bit-12	G6
	Bit-13	G7
	Bit-14	G8
	Bit-15	G9
2	Bit-16	B2
	Bit-17	B3
	Bit-18	B4
	Bit-19	B5
	Bit-20	B6
	Bit-21	B7
	Bit-22	B8
	Bit-23	B9
3	Bit-24	-
	Bit-25	-
	Bit-26	B0
	Bit-27	B1
	Bit-28	G0
	Bit-29	G1
	Bit-30	R0
	Bit-31	R1

5.0 INTERFACE SIGNAL TIMING SPECIFICATION

5.2 V by One Input Signal Timing

< Table 8. Signal Timing Table >

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Unit Interval(VBO Operation Bit Rate)	tRBIT	3byte mode	266	tTCIP/30	1667	PS
		4byte mode	266	tTCIP/40	1667	PS
		5byte mode	266	tTCIP/50	1667	PS
Eye Width at Package Pin	tREYE	-	-	0.5	-	UI
Eye Width Position A at Package Pin	tA	-	-	0.25	-	UI
Eye Width Position B at Package Pin	tB	-	-	0.3	-	UI
Eye Width Position Cat Package Pin	tC	-	-	0.7	-	UI
Eye Width Position D at Package Pin	tD	-	-	0.75	-	UI
Eye Width Position E at Package Pin	tE	-	-	0.7	-	UI
Eye Width Position F at Package Pin	tF	-	-	0.3	-	UI
Intra – pair Skew	tRISK_intra	-	-	-	0.3	UI
Inter – pair Skew	tRISK_inter	-	-	-	40	UI
SSCG	-	30KHz modulation	-0.5	-	+0.5	%



	Y[mV]
A	0
B	50
C	50
D	0
E	-50
F	-50

5.0 INTERFACE SIGNAL TIMING SPECIFICATION

5.3 Signal Timing Parameters

< Table 9. Timing Table >

Item		Symbols	Min	Typ	Max	Unit
Pixel Clock Frequency		1/Tc	69	74.25	75	MHz
Frame Rate		F	47	60(50)	61	Hz
Vertical	Total	T_V	2200	2250(2700)	2850	T_H
	Display	T_{VD}	2160			T_H
	Blank	T_{VB}	40	90(540)	690	T_H
Horizontal	Total	T_H	530	550	570	T_{CLK}
	Display	T_{HD}	480			T_{CLK}
	Blank	T_{HB}	50	70	90	T_{CLK}

Item		Symbols	Min	Typ	Max	Unit
Pixel Clock Frequency		1/Tc	69	74.25	75	MHz
Frame Rate		F	47	48	61	Hz
Vertical	Total	T_V	2200	2816	2850	T_H
	Display	T_{VD}	2160			T_H
	Blank	T_{VB}	40	656	690	T_H
Horizontal	Total	T_H	530	550	570	T_{CLK}
	Display	T_{HD}	480			T_{CLK}
	Blank	T_{HB}	50	70	90	T_{CLK}

Notes:

1.This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

2. This product should keep clock frequency and Horizontal value fixed when adjusting frame rate.

5.4 Input Signals, Basic Display Colors and Gray Scale of Colors

< Table 10. Input Signal and Display Color Table >

Color		Input Color Data																													
		MSB RED LSB										MSB GREEN LSB										MSB BLUE LSB									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

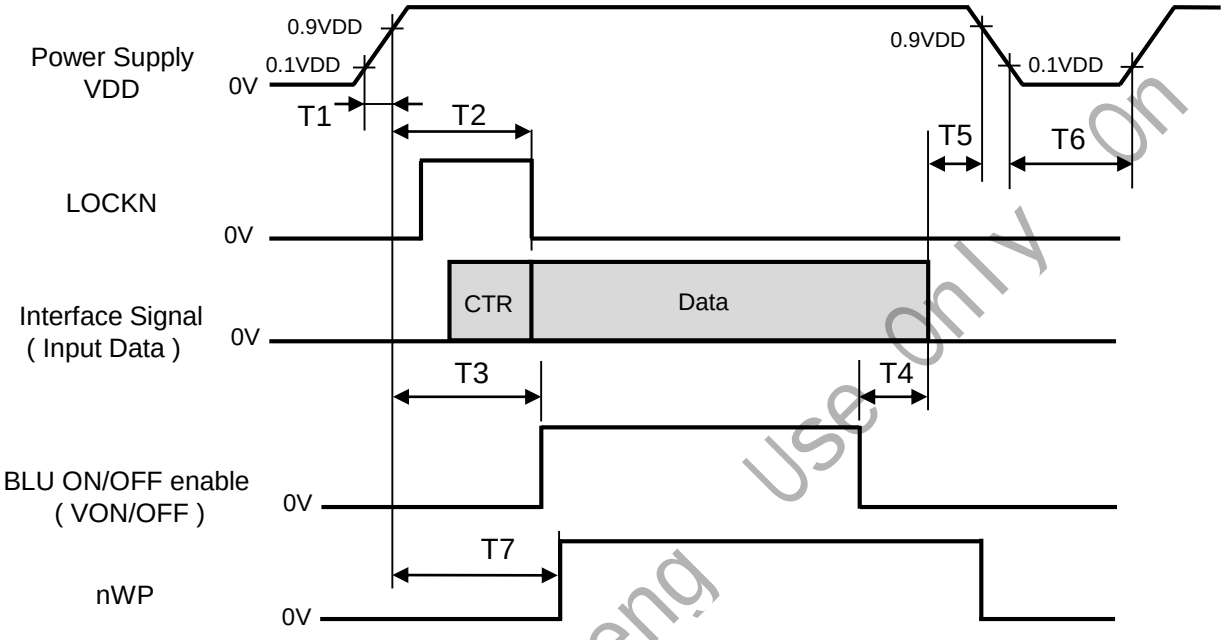
	RED(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	Green (000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
B	Blue(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	Blue(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

5.5 Power Sequence

In order to get a normal display of the Open Cell, the power on/off sequence shall be as shown in below.



< Table 11. Sequence Table >

Parameter	Values			Units
	Min	Typ	Max	
T1	0.5	-	10	ms
T2	0	-	500	ms
T3	T2	-	-	-
T4	100	-	-	ms
T5	0	-	-	ms
T6	1	-	-	s
T7	T3	-	-	-

Notes: 1. Even though T1 is out of SPEC, it is still ok if the inrush current of VDD is below the limit.

2. Back Light enable must after power ready for logic and interface signal are valid.

3. All input signals should set to 0 volt before VDD rising edge ready.

4. If possible, T3 should not less than hundreds of milliseconds, so do T2.

5. nWP pull high should be after BLU enable. Avoid conflicts when SOC and Tcon use the same IIC channel at the same time.

6. VDD should rise and fall smoothly. If there is rebounding voltage when falling stage, it must smaller than 5 volts.

6.0 OPTICAL SPECIFICATION

The test of optical specifications shall be measured in a dark room (ambient luminance≤1 lux and temperature=25±2℃) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 180cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to $\theta_{Ø=0}$ (=θ_3) as the 3 o'clock direction (the "right"), $\theta_{Ø=90}$ (= θ_{12}) as the 12 o'clock direction ("upward"), $\theta_{Ø=180}$ (= θ_9) as the 9 o'clock direction ("left") and $\theta_{Ø=270}$(= θ_6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 12.0V +/-10% at 25°C. Optimum viewing angle direction is 6 'clock.

< Table 12. Optical Table >

[VDD = 12.0V, Frame rate = 60Hz, Ta =25±2 ℃]

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	Θ_3	CR > 10	-	89	-	Deg.	Note1
		Θ_9		-	89	-	Deg.	
	Vertical	Θ_{12}		-	89	-	Deg.	
		Θ_6		-	89	-	Deg.	
Contrast ratio		CR		900:1	1200:1	-		Note2
Reproduction of color	White	W_x	Θ = 0° (Center) Normal Viewing Angle	TYP. - 0.03	0.279	TYP. + 0.03		Note3
		W_y			0.308			
	Red	R_x			0.636			
		R_y			0.333			
	Green	G_x			0.299			
		G_y			0.619			
	Blue	B_x			0.154			
		B_y			0.060			
Response Time	G to G	T_g		-	8	10	ms	Note4
Cell Transmittance				4.59	5.1	-	%	Note5
Gamma Scale				2.0	2.2	2.4		

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of $\theta = 0°$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See Figure 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in this table shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel. The chromaticity coordinates are based on BOE backlight.
4. Response time Tg is the average time required for display transition by switching the input signal as below table and is based on Frame rate fV = 60Hz with BOE Tcon Board to optimize. Each time in below table shall be measured by switching the input signal for "any level of gray(bright)"and "any level of gray(dark)"

Measured Response Time		Target																
		0	15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255
Start	0																	
	15																	
	31																	
	47																	
	63																	
	79																	
	95																	
	111																	
	127																	
	143																	
	159																	
	175																	
	191																	
	207																	
	223																	
	239																	
	255																	

5. Definition of Transmittance (T%) :
   Module is with white(L255) signal input

$$\text{Transmittance} = \frac{\text{Luminance of LCD Module}}{\text{Luminance of BLU}} \times 100\ \%$$

7.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

< Table 13. Reliability Test Parameters >

No	Test Items	Conditions
1	High temperature storage test	Ta = 60 ℃, 240 hrs
2	Low temperature storage test	Ta = -20 ℃, 240 hrs
3	High temperature & high humidity operation test	Ta = 50 ℃, 80%RH, 240hrs
4	High temperature operation test	Ta = 50 ℃, 240hrs
5	Low temperature operation test	Ta = -5 ℃, 240hrs
6	Thermal shock	Ta = -20 ℃ ↔ 60 ℃ (0.5 hr), 100 cycle
7	Open cell vibration test	1.05G,5-200Hz,Random,+Z,1Hour

Note : Test condition is based on BOE module.

8.0 PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD Open Cell.

8.1 Precautions when taking out the Panel

- Pick the pouch only, when taking out panel from a shipping package.
- Recommend to use suitable sucker to pick up and put down panel.

8.2 Precautions for handling the panel

- As the electrostatic discharges may break the LCD panel, handle the LCD panel with care. Peel a protection sheet off from the LCD panel surface as slowly as possible. Refer to the appendix 3.
- As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD panel should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Put the panel display side down on a flat horizontal plane.
- Handle connectors and cables with care.

8.3 Precautions for the operation

- The LCD product shall be operated under normal conditions as below:
  - VDD: 12±0.12V
  - Temperature: 20±15℃
  - Humidity: 55±20%
  - Display pattern: continually changing pattern(Not stationary)
- Product reliability and functions are only guaranteed when the product is used under right operation usages. If product will be used in extreme conditions such as high temperature, high humidity, high altitude, special display patterns, long time operation, outdoor operation, etc.., it is strongly recommended to contact BOE for the advice about the application of engineering. Otherwise its reliability and function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock markets, and controlling systems.
- Do not exceed the absolute maximum rating value.
- Periodical power-off or screen save is needed after long-term display.

8.0 PRECAUTIONS

- Do not insert or pull out the interface connector while the LCD panel is operating.
- LCD Response time depends on the temperature.(In lower temperature, it becomes longer)
- Ensure all input signals and power supplies are complete and valid when the panel is operating. Otherwise the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the panel would be damaged. Specially, pay attention to the turn on and off sequence.

8.4 Precautions for the atmosphere

- Recommend storage atmosphere

ITEM	UNIT	MIN	MAX
Storage Temperature	(℃)	5	40
Storage Humidity	(%RH)	35	75
Storage Life	6 months		
Storage Condition	• The storage room should be equipped with a dark and good ventilation facility. • Prevent products from being exposed to the direct sunlight, moisture and water. • The product need to keep away from organic solvent and corrosive gas. • Be careful for condensation at sudden temperature change. • Storage condition is guaranteed under packing conditions.		

- Dew drop atmosphere should be avoided. When expose to drastic fluctuation of temperature (hot to cold or cold to hot) , the LCD module may be affected. Specifically, drastic temperature fluctuation from cold to hot, produces dew on the LCD module ' s surface which may affect the operation of the polarizer and LCD module.
- Do not store and/or operate the LCD panel in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

8.5 Precautions for the panel characteristics

- Do not apply fixed pattern data signal to the LCD panel at product aging.
- Applying fixed pattern for a long time may cause image sticking.

8.0 PRECAUTIONS

8.6 Other precautions

- In particular in winter, Before putting Panel boxes on the line, aging process is required to make the temperature of products similar to the temperature of workplace.
- Do not disassemble and/or re-assemble LCD panel.
- Do not re-adjust variable resistor or switch etc.
- Product assembled into module should be stored in the bag(cover case).
- Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- Be careful not to give any extra mechanical stress to the panel when designing the set, and backlight.
- Do not pull, fold or bend the source COF and the gate COF in any processes.
- If the liquid crystal material leaks from the panel, this should be kept away from the eyes or mouth. If this contacts to hands, legs, or clothes, you must washed it away with soap thoroughly and see a doctor for the medical examination.
- When returning the module for repair or etc., Please pack the module not to be broken. We recommend to use the original shipping packages.

9.0 CRITICAL COMPONENT

NO.	Printed Wire Board(S-PWB)	
1	Company name	SUNTAK MULTILAYER PCB CO LTD
2	UL file number	E207844
3	Type designation	STM-9
4	Factory identification(if PWB is produced at more than one location)	-
5	Burning Test classification	94V-0
6	Others marking information as mentioned in individual E-File number	

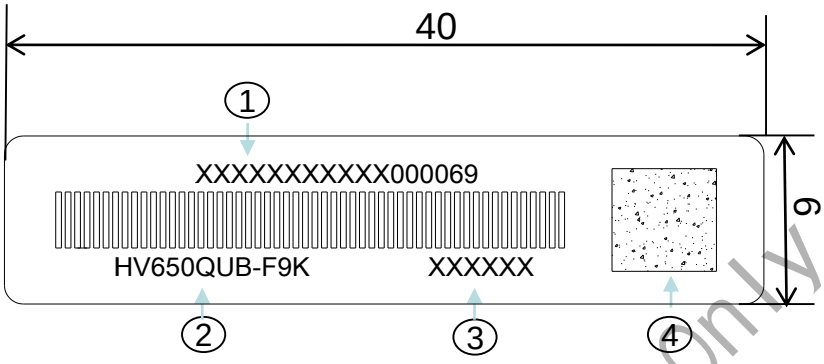
NO.	Printed Wire Board(S-PWB)	
1	Company name	ELEC & ELTEK MULTILAYER PCB LTD
2	UL file number	E54926
3	Type designation	E3330HF4
4	Factory identification(if PWB is produced at more than one location)	-
5	Burning Test classification	94V-0
6	Others marking information as mentioned in individual E-File number	

9.0 CRITICAL COMPONENT

NO.	Printed Wire Board(C-PCB)	
1	Company name	SUNTAK MULTILAYER PCB CO LTD
2	UL file number	E207844
3	Type designation	STM-9
4	Factory identification(if PWB is produced at more than one location)	-
5	Burning Test classification	94V-0
6	Others marking information as mentioned in individual E-File number	

NO.	Printed Wire Board(C-PCB)	
1	Company name	ELEC & ELTEK MULTILAYER PCB LTD
2	UL file number	E54926
3	Type designation	E3330HF4
4	Factory identification(if PWB is produced at more than one location)	-
5	Burning Test classification	94V-0
6	Others marking information as mentioned in individual E-File number	

9.0 PRODUCT SERIAL NUMBER



Item	Size(mm)
Label	40*9
QR code	5.5*5.5

Remark:
1. MDL ID
2. FG Code
3. Date
4. QR Code

MDL ID Naming Rule:

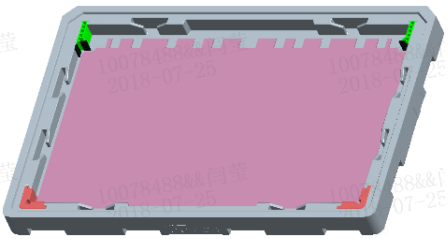
Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Code	S	L	S	9	1	6	3	5	9	4	2	0	A	A	0	0	0
Description	Model Code /GBN		Grade	Line	Year		Month	Model Extension Code (Last 4 Digits Of FGCOD)				Serial No 00001-ZZZZZZ					

10.0 PACKING INFORMATION

BOE provides the standard shipping container for customers, unless customer specifies their packing information. The standard packing method and Barcode information are shown in below.

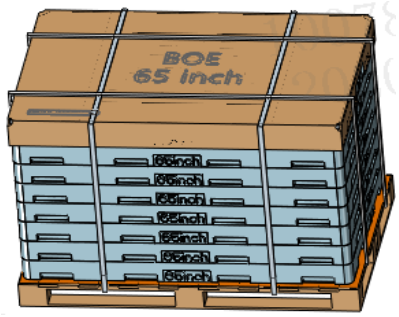
10.1 Packing Order

Put EPE pads and panels into the box, 12pcs panels per box and 13pcs EPE pads per box



Put the box on the pallet, 8ea boxes per pallet

京东方科技集团股份有限公司
BOE TECHNOLOGY GROUP CO.,LTD.



Put one Paper cover on the top of boxes , pack with wrapping film & belts

Cautions :

When transferring in warehouse or factory, the arm length of electric forklift or hand pallet truck must be longer than the pallet along the insertion direction.

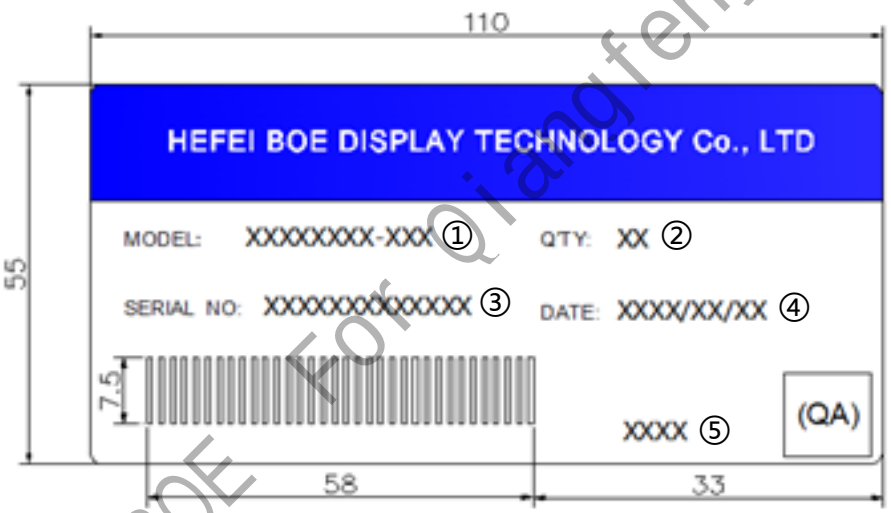
10.2 Packing Note

Item	Size(mm)	Weight(Kg)	Material
Desiccant	210*80	0.04	$CaCl_2$
Box	1640(±6)*1090(±5)*128(±1.5)	6.269	EPO
Pallet	1690*1140*137	24	Wood
Pallet Packing	1690*1140*1110	419.561	-

10.3 Box Label

- Label Size : 110 mm (L) × 55 mm (W)
- Contents

  Model : HV650QUB-F9L
  Q`ty : 12 Open Cell in one box.
  Serial No. : Box Serial No. See next page for detail description.
  Date : Packing Date
  FG Code : FG Code of Product



Remark:

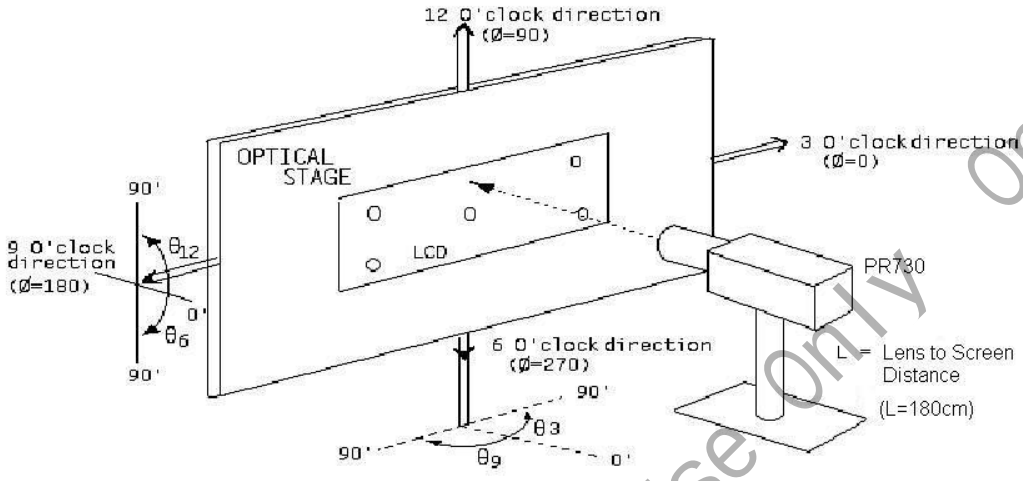
1. FG-CODE Number
2. Quantity in one box
3. Box ID
4. Packing Date
5. FG-Code Last Four Number

Total Size:110×55mm

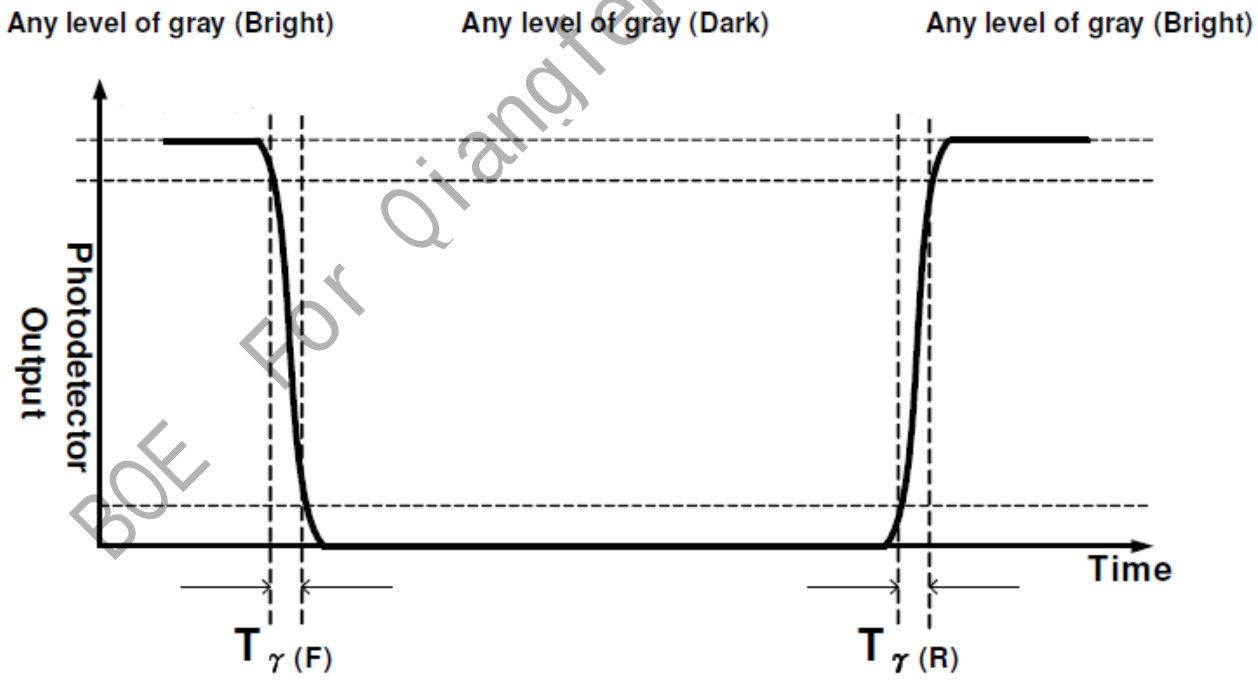
Box ID Naming Rule:

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Code	S	L	S	9	1	6	3	5	9	4	2	0	0
Description	Products GBN		Grade	Line	Year		Month	Revision Code	Serial No 00001-ZZZZZZ				

11.0 APPENDIX 1

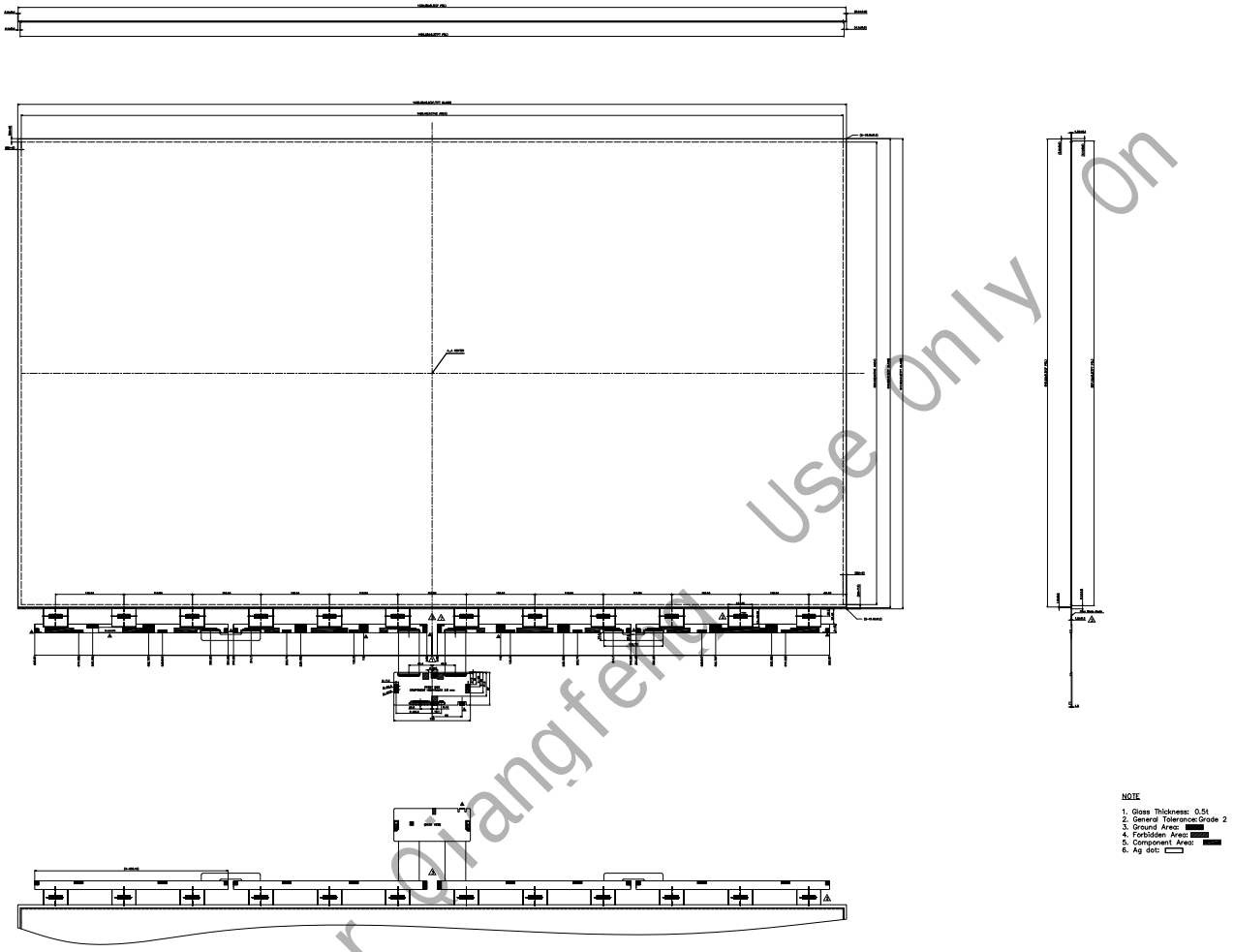


< Figure 1. Measurement Set Up >



< Figure 2. Response Time Testing >

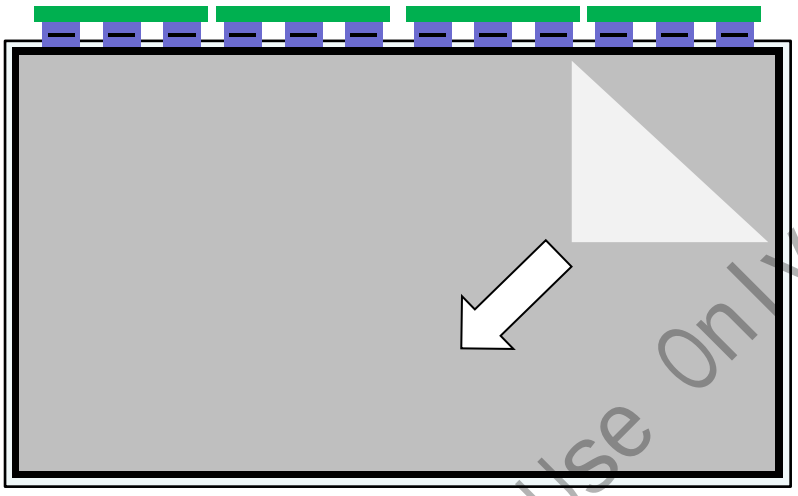
11.0 APPENDIX 2



< Figure 3. TFT-LCD Open Cell Outline Dimensions (Front View) >

TOLERANCE TABLE(±)				
DIMENSION	1 GRADE	2 GRADE	3 GRADE	4 GRADE
L ≤ 20	0.05	0.1	0.1	0.2
20 < L ≤ 50	0.1	0.15	0.2	0.25
50 < L ≤ 100	0.15	0.2	0.25	0.3
100 < L ≤ 200	0.2	0.25	0.3	0.5
200 < L	0.25	0.3	0.5	0.8
UNLESS OTHERWISE SPECIFIED				

11.0 APPENDIX 3



< Figure 4. TFT POL Protect Film Peeling Method >

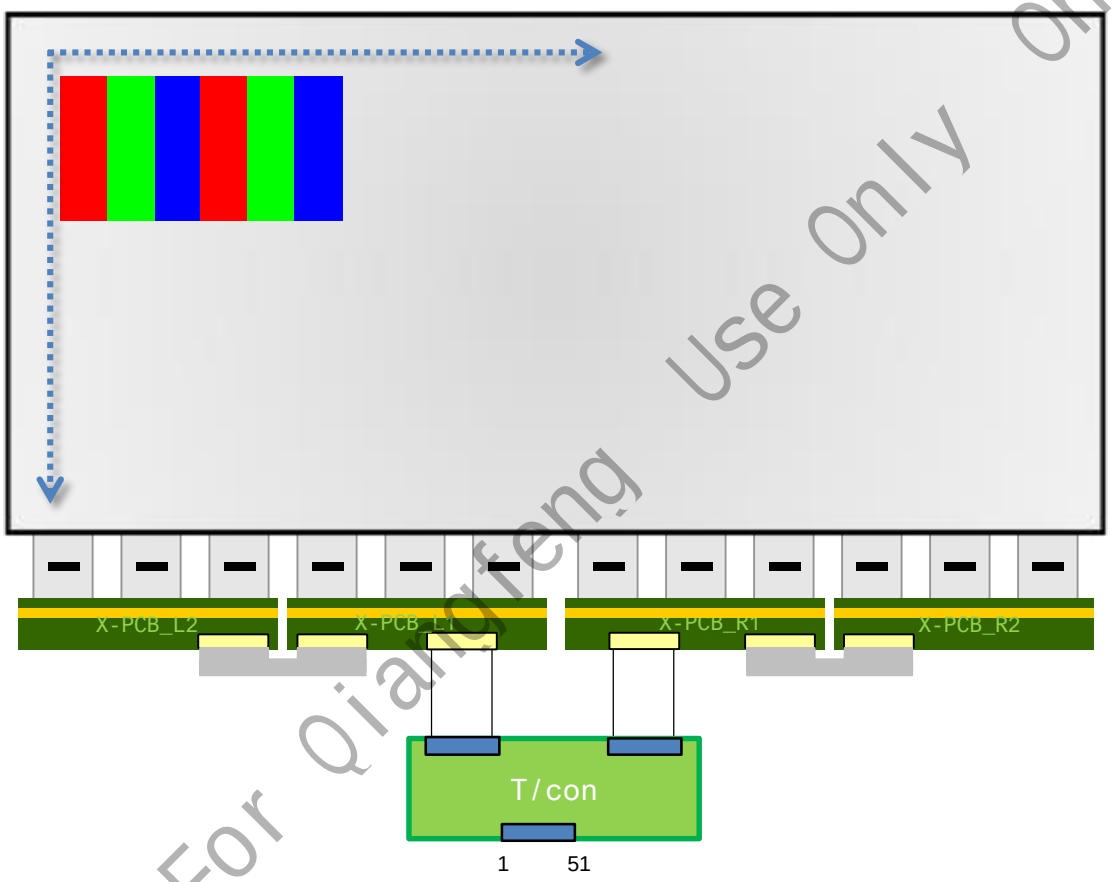
Peeling Steps:

1. Be sure to peel off slowly(recommended more than 7sec) and constant speed.
2. Peeling direction shows in Figure 4.
3. Be sure to ground person with adequate methods such as the anti-static wrist band.
4. Be sure to ground each source PCB while peeling off the protection film.
5. Ionized air should be blown over during peeling action.
6. The protection film must not touch drivers and source PCBs.
7. If adhesive may remain on the polarizer after the protection film peeling off, please remove with isopropyl-alcohol.

Note: COFs and PCBs show product outer contour only in the above diagram. Focus on the peeling step and ignore the number of COFs and size of PCBs.

11.0 APPENDIX 4

This product is reverse type display. RGB data mapping scan direction : from left-up to right-down.



< Figure 5. Display Mode>

Note: COFs and PCBs show product outer contour only in the above diagram. Focus on the scan direction and ignore the number of COFs and size of PCBs.

11.0 APPENDIX 5

< Figure 6. EDID Table>

EPH2 65”

■ EEPROM(24C256) slave address :AA (1010 1010)

No.	Item	Spec	Address	Data	Remarks
1	Part Number	**YSDM009CCO0101**	E0~EF	59,53,44,4D,30,30,39,43, 43,4F,30,31,30,31,00,00	

EEPROM data map

	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
00	F2	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
10	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
20	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
30	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
40	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
50	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
60	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
70	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
80	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
90	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
E0	59	53	44	4D	30	30	39	43	43	4F	30	31	30	31	00	00
F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

BOE

No.12 Xihuanzhong Road BDA Beijing, 100176, P.R. China

Declaration of Red Phosphorus Fire Retardants Free

Model No : HV650QUB-F9L

We herewith confirm that the display product delivered by BOE do not contain Red Phosphorus Fire Retardants.

Date	2022.09.27
Company	BOE Technology Group Co. Ltd
Department	Quality System Department
E-mail	wuxianping@boe.com.cn
Signature