MODEL: ST4251D02-3

Ver. : 2.1

Date: 15.Dec.2023

Customer's Approval	**CSOT**
Signature Date	Approved By Product Director Date Name: Signature:
	Reviewed By PM Manager Date Name: Signature:
	Reviewed By Project Leader Date Name: Signature:
	Reviewed By PM Date Name: Signature:

Contents

Revision History

Version	Date	Page (New)	Section	Description	Revision by
Ver. 0.1	Dec 31,2021	All	All	Tentative Specification was First Issued	Hanxian Liu
Ver. 0.2	Nov 18,2022	Page31,34	8.2.2; 10.1	Update datails	Zhiming Cheng
Ver. 0.3	Dec 12,2022	Page30	8.1.1	Update Mechanical Specification	Zhiming Cheng
Ver. 0.4	Dec 23,2022	Page6, 26	1.3; 7.2	Update Color Chromaticity & Gray scale	Zhiming Cheng
Ver. 0.5	Jan 3,2023	Page 5, 6, 26	1.1; 1.3; 7.2	Update CR	Zhiming Cheng
Ver. 0.6	Feb 6,2023	Page 10, 11, 26	3.1.2; 3,1,3; 7.2	Update Power design current demand, Power consumption And CR Min.	Zhiming Cheng
Ver. 0.7	Mar 3,2023	Page 6,19	1.3; 6.1.2	Update General information , GOA OCP setting.	Lijiao Tan
Ver. 0.8	Apr 4,2023	Page 9, 31	3.1.1;8.2.1	Update Open Cell DC voltage and ripple; Update weight in Packing Specifications	Zhiming Cheng
Ver. 2.1	Apr 6,2023	Page 7, 17, 34	2.2;10.3;5.	Update Environment Requirement; Update reliability test items and conditions; Update power on/off sequence	Zhiming Cheng
Ver. 2.1	Dec 15,2023	Page 6, 26	1.3;7.2.	Update Color Chromaticity and Gray scale of Optical Specifications.	Zhiming Cheng

1. General Description

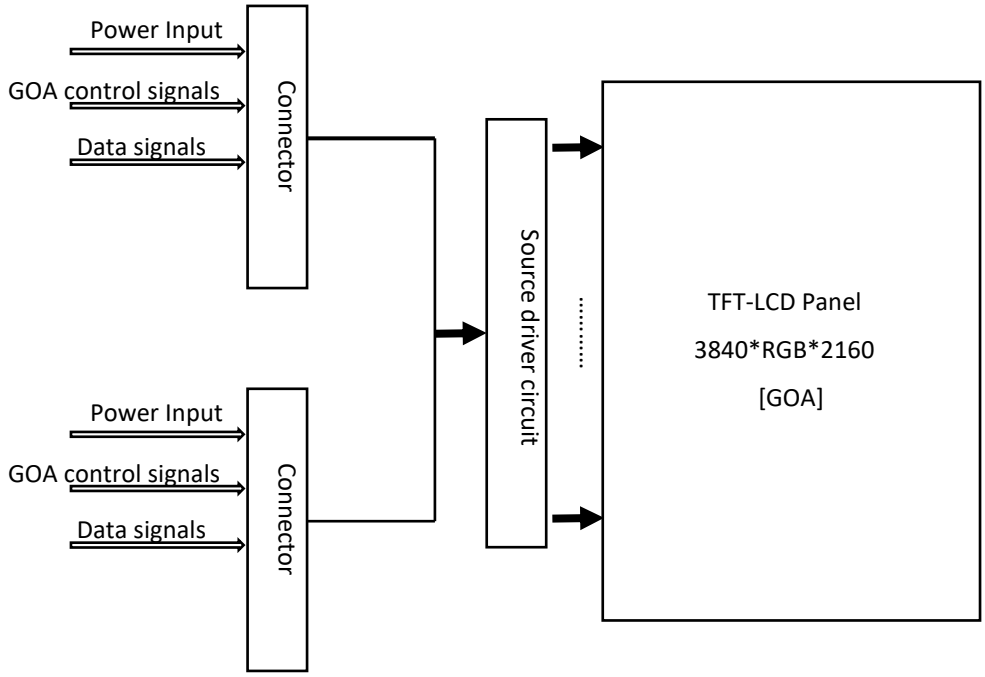
1.1 Product Features

- **QFHD Resolution (3840 x 2160)**
- **Very High Contrast Ratio: 4000:1**
- **Fast Response Time**
- **High Frame Rate:60Hz**
- **High Color Saturation: NTSC 72%(CSOT BLU)**
- **Ultra Wide Viewing Angle**
- **CEDS interface**

1.2 Overview

ST4251D02-3 is a diagonal 42.5” color active matrix open cell. This open cell is a transmissive type display operating in the normally black mode. It supports 3840x2160 QFHD resolution and can display up to 1.07G colors (8bit+FRC). Each pixel is divided into Red, Green and Blue sub-pixels which are arranged in vertical stripe.

This open cell dedicates for LCD TV products and provides excellent performance which includes high brightness, ultra wide viewing angle, high color saturation and high color depth. CSOT open cell comply with ROHS for identification.



1.3 General Information

Item	Specification	Unit	Note
Active Area	941.1840 (H)x529.4160 (V)	mm	
Cell Size	953.0(H)x 543.0(V)	mm	
Weight	1.63	kg	
Driving Scheme	a-Si TFT Active Matrix	-	
Number of Pixels	3840x2160	pixel	
Pixel Pitch (Sub Pixel)	81.7(H)x 245.1(V)	um	
Pixel Arrangement	RGB Vertical Stripe	-	
Display Colors	1.07G	color	8bit+FRC
Display Mode	Transmissive Mode, Normally Black	-	
Glass Thickness (Array/CF)	0.5/0.5	mm	
Color Chromaticity	Red(0.639,0.336) Green (0.296,0.616) Blue (0.150,0.063) White(0.272 ,0.311)		Typical value measured at CSOT's ST4251D02-3
Contrast Ratio	4000:1		
Cell Transmittance	4.3 %(Typ.)(CSOT BLU)	%	
View Angle(CR>10)	178° (H)/178° (V)		
Surface Treatment	Anti-Glare, Haze 2%， Hard Coating(3H) –CF POL		POL

2. Absolute Maximum Ratings

2.1 Absolute Maximum Ratings (Ta = 25 ± 2 °C)

The followings are maximum values which, if exceeded, may cause damage to the unit.

Item	Symbol	Value		Unit
		Min.	Max.	
Digital Supply Voltage	VDD1V8	-0.3	2.5	V
Digital Supply Voltage	VDD3V3	-0.3	3.6	V
Analog Supply Voltage	AVDD	-0.3	19.8	V

2.2 Environment Requirement

(1) Temperature and relative humidity range are shown as below

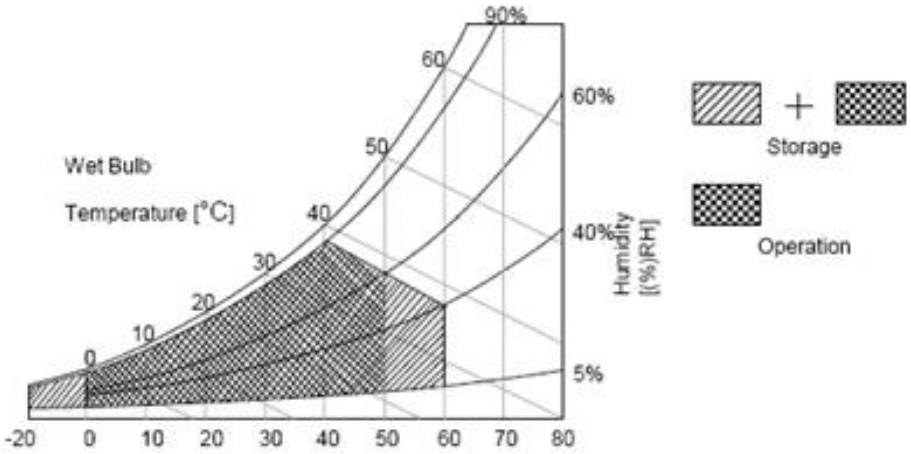


Fig. 2.1 Operating and storage environment

(a) 90%RH maximum (Ta ≤ 39ºC).

(b) Wet-bulb temperature should be 39ºC maximum (Ta > 39ºC).

(c) No condensation.

(2) The storage temperature is between -20 ºC to 60 ºC, and the operating ambient temperature is between 0 ºC to 50 ºC. The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65ºC with LCD module in a temperature controlled chamber alone. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65ºC. The range of operating temperature may degrade in case of improper thermal management in the end product design.

(3) The rating of environment is based on LCD module. Leave LCD cell alone, this environment condition can't be guaranteed. Except LCD cell, the customer has to consider the ability of other parts of LCD module and LCD module process.

2.3 Package Storage

When storing open cell as spares for a long time, please follow the precaution instructions:

(1) Do not store the open cell in high temperature and high humidity for a long time. It is highly recommended to store the open cell with temperature from 5ºC ~ 40ºC and humidity from 35%RH ~ 75%RH with shipping package.

(2) The open cell should be keep at a circumstance shown below:

0-2months	2-3months	3-6months
No baking	50℃、10%RH，24hr	50℃、10%RH，48hr

3. Electrical Specification

3.1 Electrical Characteristics

3.1.1 Open Cell DC voltage and ripple (Ta =25 ± 2ºC)

Parameter	Symbol	Value			Ripple	Note
		Min.(V)	Typ.(V)	Max.(V)	Pk-Pk (mV)	
Analog power supply	VAA	13.6	13.9	14.2	+/-5%	(1)
Digital power supply	VDD1V8	1. 7	1.8	1.9	+/-5%	
Power supply for CML	VTERM	1.0	1.2	1.3	+/-5%	
Power supply for Gate on output	VGHF	29. 5	30	30.5	/	(1) (3)
Power supply for Gate off output	VGL	-10.3	-10	-9.7	/	
Power supply for Gate off output	VSSQ	-10.3	-10	-9.7	+/-5%	(1)
Power supply for Gate off output	VSSG	-6.3	-6	-5.7	+/-5%	
Power supply for flash	VDD33	3.1	3.3	3.5	+/-5%	
Power supply for array Vcom	CFVCOM	4.23	4.43	4.62	+/-1%	
	AVCOM	4.22	4.42	4.62	+/-1%	
Power supply for source IC	HVAA	6.15	6.45	6.75	+/-5%	(1) (2)
Gamma voltage	GMA1~GMA9	HVAA+0.2	-	VAA-0.2	150	
	GMA10~GMA18	0.2	-	HVAA-0.2	150	(1) (4)
	GMA1	12.93	13.08	13.23	150	
	GMA3	10.73	10.88	11.03	150	
	GMA5	9.59	9.74	9.89	150	
	GMA7	9.03	9.18	9.33	150	
	GMA9	7.09	7.24	7.39	150	
	GMA10	5.57	5.72	5.87	150	
	GMA12	3.83	3.98	4.13	150	
	GMA14	3.04	3.19	3.34	150	
	GMA16	1.71	1.86	2.01	150	
	GMA18	0.08	0.23	0.38	150	

Note:

(1) Measurement condition: Ta = 25 ± 2ºC, F = 60Hz. The test patterns are shown as below. All the ripple voltage is measured on XB PCBA.

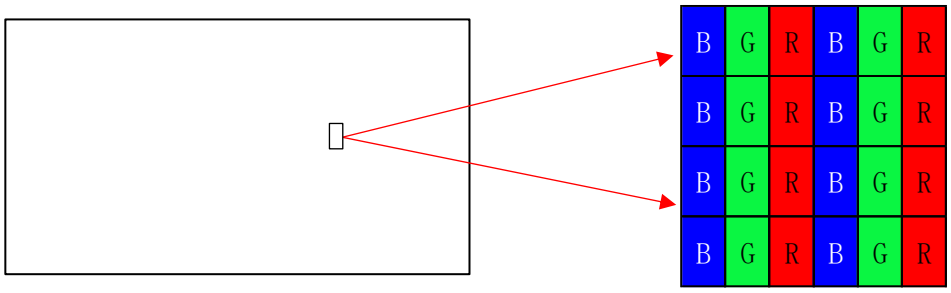
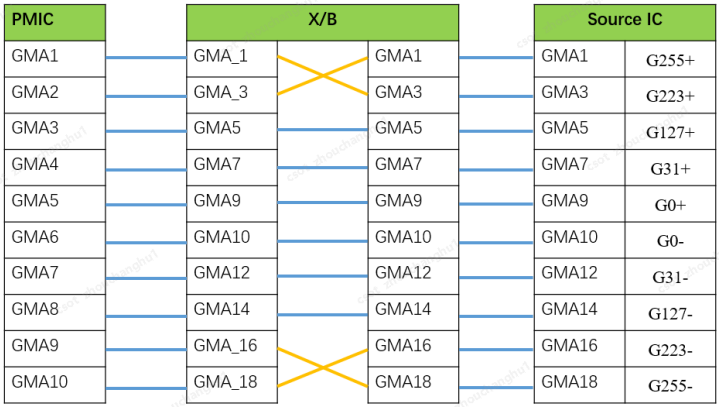


Fig. 3.1 White pattern

(2) HVAA must be: GM6+0.2V<HVAA<GM5-0.2V

(3) The value of VGHF, VGL ripple just refer to CSOT design.

(4) Gamma order is reversed only on the X/B which shows as below, but it doesn't influence the order on the SoC. The purpose is to provide auto gamma program algorithm with easy implementation



3.1.2 Power design current demand

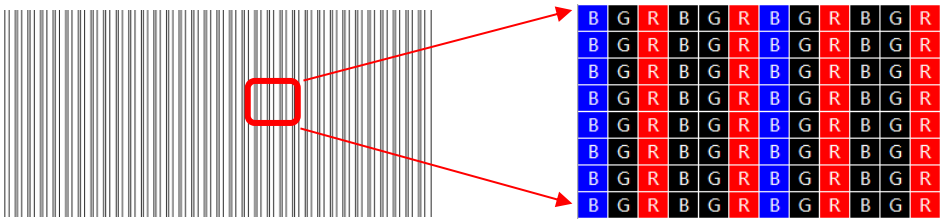
Symbol	Min	Unit	Note
I_{VAA}	600	mA	
I_{VDD18}	300	mA	
I_{VTERM}	50	mA	
I_{CK}	40	mA	One of CK
I_{VSS}	30	mA	
I_{VDD33}	50	mA	
I_{AVCOM}	20	mA	
I_{CFVCOM}	20	mA	
I_{HVAA}	200	mA	

Note:

(1) The above data are recommended values for your reference only

3.1.3 Power consumption

Heavy load pattern



Parameter	Symbol	Min	Type	Max	Unit
Power consumption	PDD	-	18	24	W
Power Supply Current	IDD	-	1500	2000	mA

Note：Power consumption & current were measured by Tcon board. Input voltage was 12.0V.

3.1.4 CEDS Differential Signal Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Driver IC Clock frequency	Freq	1200	-	3050	Mbps	-
input offset voltage	VCM ceds	0.65	-	VCC-(VID)/2	V	(1)
SSCG Modulation Ratio	SS%	-2	-	+2	%	(2)
SSCG Modulation Frequency	fSS	-	-	100	KHz	(2)
Parameter	Symbol	Normalized Time		Differential Amplitude		-
Absolute Eye-Diagram Mask	A	0.25	UI	0	UI	VDD18 = 1.62~1.98V CDR Bandwidth = 5MHz Damping factor = 0.7V
	B	0.5	UI	75	mV	
	C	0.75	UI	0	UI	
	D	0.5	UI	-75	mV	

Note:

(1) $VCMceds=(V_{CEDS(P)}+ V_{CEDS(N)})/2$

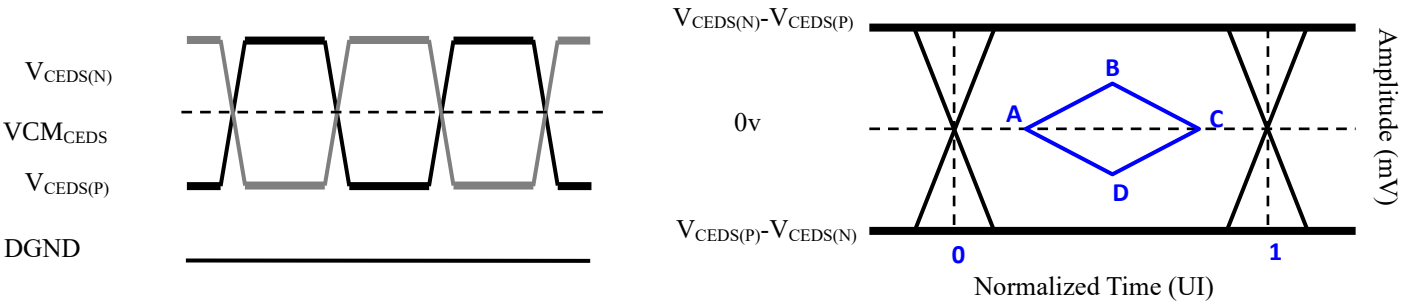


Fig. 3.2 CEDS signal definition

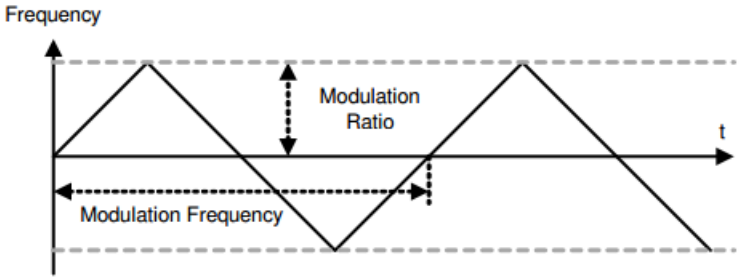


Fig. 3.3 SSCG modulation by modulating clock period

Note:

(2) Recommend SSCG M/R & SSCG MF as follow：

SSCG Modulation Ratio	-
SSCG Modulation Frequency	-

When modulation freq.<50KHz, Modulation ratio is ±2.0%

When modulation freq.=50KHz~100KHz, Modulation ratio = ±(3 – 0.02*Fmod). (Fmod unit is KHz)

SSC modulation frequency	SSC modulation ratio (%)
~ 50KHz	+/- 2.0%
60KHz	+/- 1.8%
70KHz	+/- 1.6%
80KHz	+/- 1.4%
90KHz	+/- 1.2%
100KHz	+/- 1.0%

3.2 Driver IC ESD spec

The Electro-Static Discharge tolerance of Source COF IC is +-2KV tested by ESD Gun. Especially if the LCD module is designed with the Plastic Bezel, ESD protection solutions should be applied to avoid damaged, as shown in Fig.3.4.

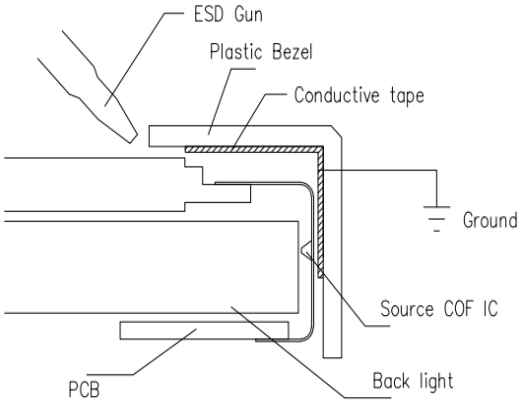


Fig. 3.4 Source COF IC ESD protection

3.3 Driver IC Temperature spec

Parameter	Symbol	SPEC			Unit	Note
		Min.	Typ.	Max.		
Surface temperature	Tc	-	-	120	℃	(1)

Note:

Any point on the IC surface must be less than maximum spec under any conditions, if the surface temperature is out of the spec, thermal solutions should be applied to avoid the damage. The IC surface temperature is measured at room temperature of 25℃.

4. Input Terminal Pin Assignment

4.1 Interface Pin Assignment

CN: 6-05192101-0 (XDYT) or equivalent

Source PCB XR pin define				Source PCB XL pin define			
Pin No.	Symbol	Description	Note	Pin No.	Symbol	Description	Note
1	NC	No Connection		1	CLK1	Clock input for GOA circuit	
2	NC	No Connection		2	CLK2	Clock input for GOA circuit	
3	NC	No Connection		3	CLK3	Clock input for GOA circuit	
4	NC	No Connection		4	CLK4	Clock input for GOA circuit	
5	GND	Ground		5	CLK5	Clock input for GOA circuit	
6	GMA_18	Gamma voltage 18		6	CLK6	Clock input for GOA circuit	
7	GMA_16	Gamma voltage 16		7	CLK7	Clock input for GOA circuit	
8	GMA14	Gamma voltage 14		8	CLK8	Clock input for GOA circuit	
9	GMA12	Gamma voltage 12		9	NC	No Connection	
10	GMA10	Gamma voltage 10		10	NC	No Connection	
11	GMA9	Gamma voltage 9		11	NC	No Connection	
12	GMA7	Gamma voltage 7		12	VGH_ODD(LC2)	Low frequency clock	
13	GMA5	Gamma voltage 5		13	VGH_EVEN(LC1)	Low frequency clock	
14	GMA_3	Gamma voltage 3		14	VSSQ	Power supply for analog circuit	
15	GMA_1	Gamma voltage 1		15	NC	No Connection	
16	GND	Ground		16	STV	Start Pulse for GOA circuit	
17	LOCKOUT6	LOCK signal Output		17	VSSG	Power voltage for GOA circuit	
18	GND	Ground		18	VCOM2	VCOM voltage2(4.42V)	
19	CEDS6-	Differential serial data input		19	NC	No Connection	
20	CEDS6+	Differential serial data input		20	VCOM1	VCOM voltage1(4.43V)	
21	GND	Ground		21	GND	Ground	
22	CEDS5-	Differential serial data input		22	AVDD	Power supply for analog circuit	
23	CEDS5+	Differential serial data input		23	AVDD	Power supply for analog circuit	
24	GND	Ground		24	AVDD	Power supply for analog circuit	
25	CEDS4-	Differential serial data input		25	AVDD	Power supply for analog circuit	
26	CEDS4+	Differential serial data input		26	HVDD	Power supply for source IC	
27	GND	Ground		27	VCC_18	Power supply for digital circuit	
28	NC	No Connection		28	VCC_18	Power supply for digital circuit	

29	NC	No Connection			29	VCC_12	Power supply for CML	
30	GND	Ground			30	LOCKOUT3	LOCK signal Output	
31	LOCKOUT3	LOCK signal Input			31	GND	Ground	
32	VCC_12	Power supply for CML			32	NC	No Connection	
33	VCC_18	Power supply for digital circuit			33	NC	No Connection	
34	VCC_18	Power supply for digital circuit			34	GND	Ground	
35	HVDD	Power supply for source IC			35	CEDS3-	Differential serial data input	
36	AVDD	Power supply for analog circuit			36	CEDS3+	Differential serial data input	
37	AVDD	Power supply for analog circuit			37	GND	Ground	
38	AVDD	Power supply for analog circuit			38	CEDS2-	Differential serial data input	
39	AVDD	Power supply for analog circuit			39	CEDS2+	Differential serial data input	
40	GND	Ground			40	GND	Ground	
41	VCOM1	VCOM voltage1(4.43V)			41	CEDS1-	Differential serial data input	
42	NC	No Connection			42	CEDS1+	Differential serial data input	
43	VCOM2	VCOM voltage2(4.42V)			43	GND	Ground	
44	VSSG	Power voltage for GOA circuit			44	GMA_18	Gamma voltage 18	
45	STV	Start Pulse for GOA circuit			45	GMA_16	Gamma voltage 16	
46	NC	No Connection			46	GMA14	Gamma voltage 14	
47	VSSQ	Power supply for analog circuit			47	GMA12	Gamma voltage 12	
48	VGH_EVEN(LC1)	Low frequency clock			48	GMA10	Gamma voltage 10	
49	VGH_ODD(LC2)	Low frequency clock			49	GMA9	Gamma voltage 9	
50	NC	No Connection			50	GMA7	Gamma voltage 7	
51	NC	No Connection			51	GMA5	Gamma voltage 5	
52	NC	No Connection			52	GMA_3	Gamma voltage 3	
53	CLK8	Clock input for GOA circuit			53	GMA_1	Gamma voltage 1	
54	CLK7	Clock input for GOA circuit			54	FLASH_WP	XB Flash Write Protect Input	
55	CLK6	Clock input for GOA circuit			55	FLASH_MISO	XB Flash Data Output	
56	CLK5	Clock input for GOA circuit			56	FLASH_CS	XB Flash Chip Select Input	
57	CLK4	Clock input for GOA circuit			57	FLASH_MOSI	XB Flash Data Input	
58	CLK3	Clock input for GOA circuit			58	GND	Ground	
59	CLK2	Clock input for GOA circuit			59	FLASH_CLK	XB Flash Serial Clock Input	
60	CLK1	Clock input for GOA circuit			60	VCC33	Power supply for flash	

Note:

(1) The direction of pin assignment is shown as below:

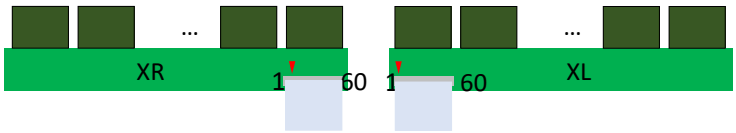
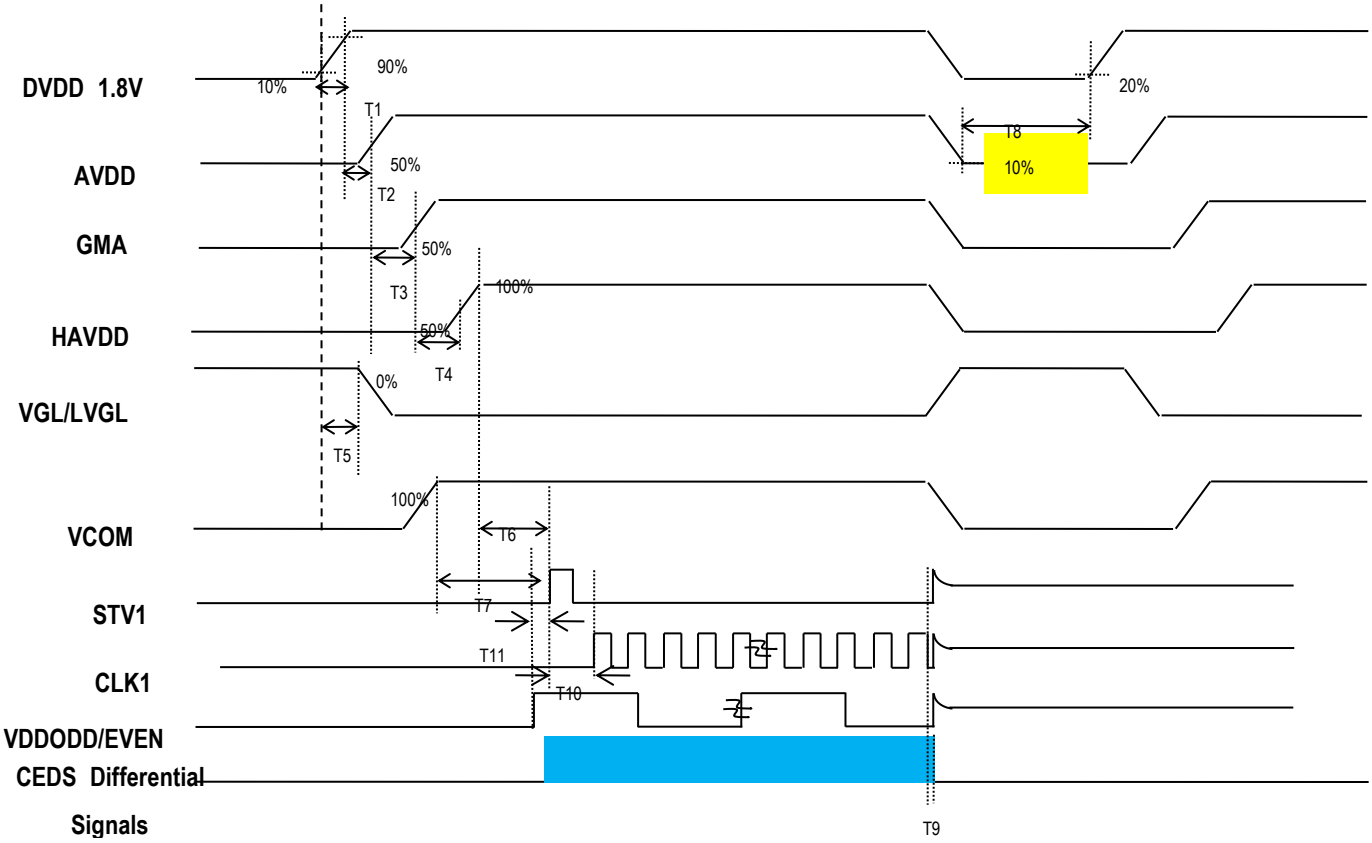


Fig. 4.1 Connector direction sketch map

(2) NC pins is for CSOT use only, please let it open.

5. Power On/off Sequence



Parameter	Values			Unit	Note
	Min.	Typ.	Max.		
T1	>0	-	10-	ms	
T2	>0	-	-	ms	
T3	>0	-	-	ms	AVDD must be higher than HAVDD and GMA all the time
T4	-200	-	1000	ms	
T5	>0	-	-	ms	
T6	>0	-	-	ms	
T7	>0	-	-	ms	
T8	1	-	-	s	
T9	>0			ms	Gate Signals must off before than Differential Signals off
T10		7.4		us	STV1 to CLKs
T11	>2			Frame	VDD rising edge to First STV1 rising edge

Note:

(1) Please keep these condition: HAVDD+0.2V< (GAM1…GAM9) <AVDD-0.2V; 0.2V<GAM18…GAM10<HAVDD-0.2V.

(2) The AVDD voltage must be higher than HAVDD& gamma all the time.

(3) Please ensure that all the signals are stable before BL on.

6. Appendix

6.1 GOA

6.1.1 60Hz GOA timing chart

Condition: H-total = 4400 V-total = 2250 Frame rate = 60 Hz

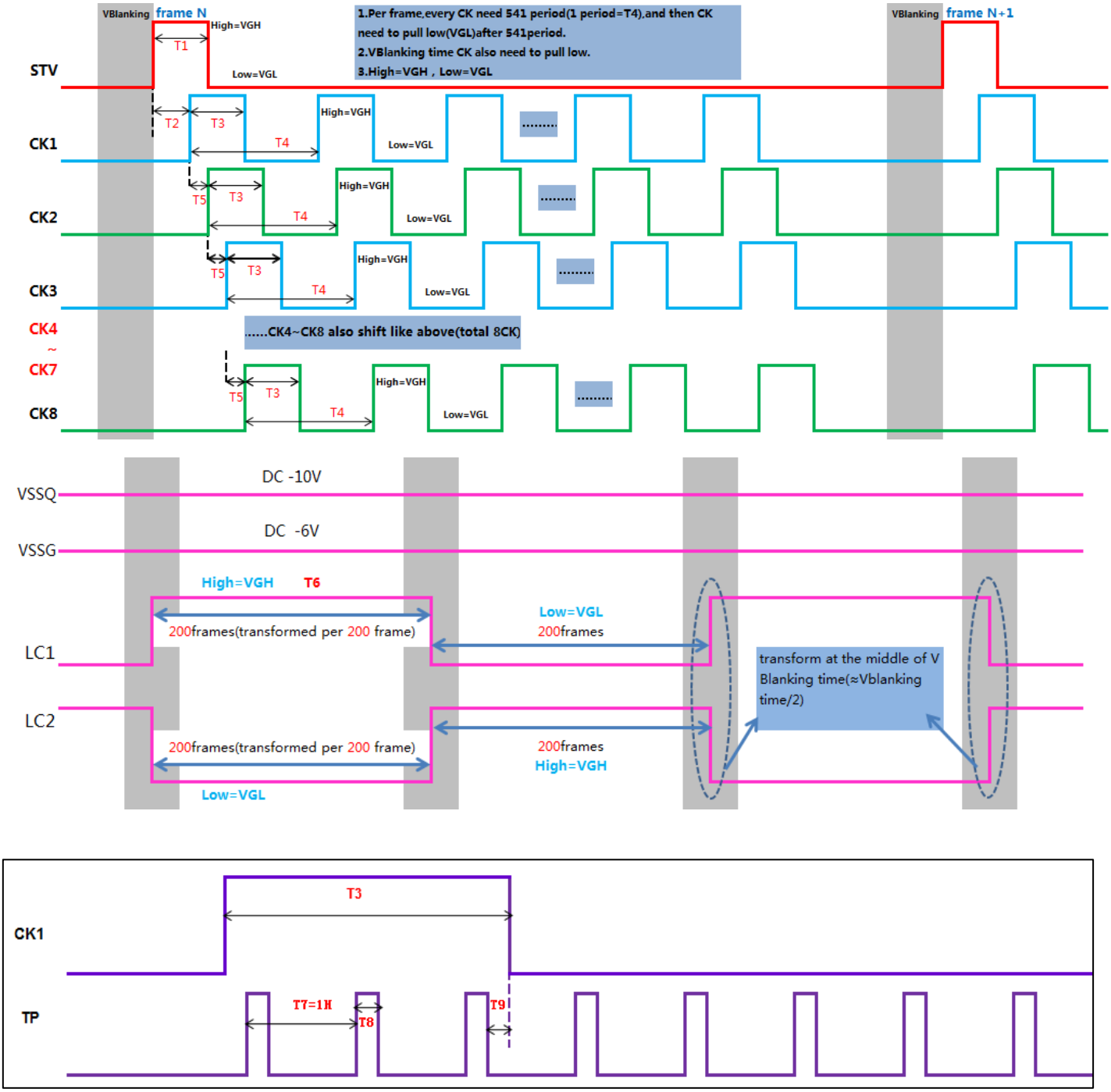


Fig. 6.1 GOA Timing chart

Parameter	Description	Value	unit	Note
T1	STV Width	18.5	us	
T2	STV raising to CK1 raising	7.4	us	
T3	CK High Width(0.4*8H)	11.84	us	
T4	CK Width(8H)	29.6	us	
T5	CK1 raising to CK2 raising (1H)	3.7	us	
T6	LC High/Low Width(200 Frame)	3.334	s	
T7	TP width(1H)	3.7	us	
T8	TP high Width	0.5	us	
T9	TP falling to CK1 falling	2.17	us	

Table 6.1 GOA timing table

6.1.2 GOA OCP setting

Note: The data is the SW50222 recommend setting.

OCP Setting	Setting Current		delay time	
	Value	Unit	Value	Unit
STV	50	mA	5	us
CK1-CK8	50	mA	7.5	us
LC1-LC2	50	mA	100	us

Table 6.2 OCP setting table

6.2 VCOM Adjustment pattern

The CSOT Flicker adjusted the pattern was show as below. if customer need below pattern please directly contact with account FAE.

■Column inversion（L127）

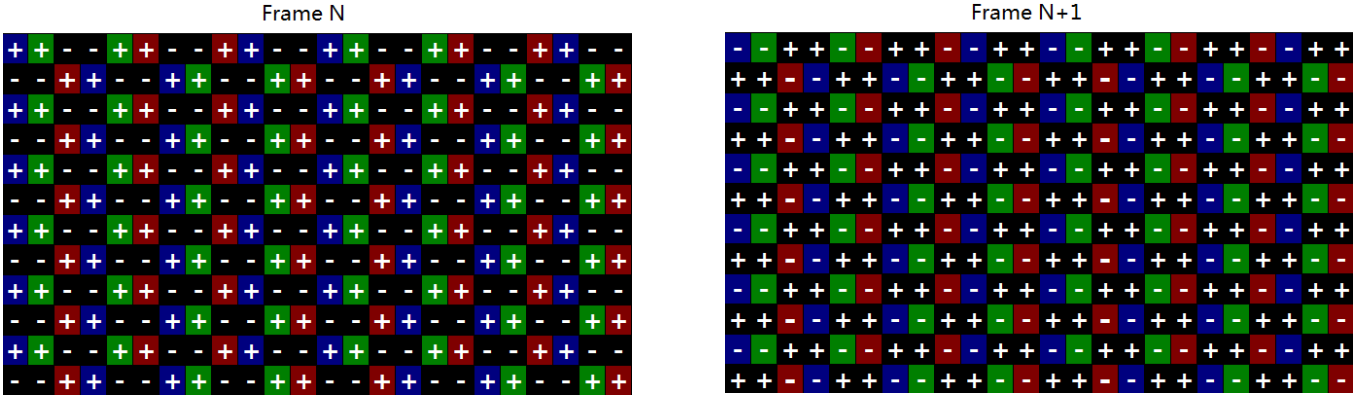


Fig. 6.2 Flicker pattern

6.3 Cell structure & data mapping

6.3.1 Cell structure

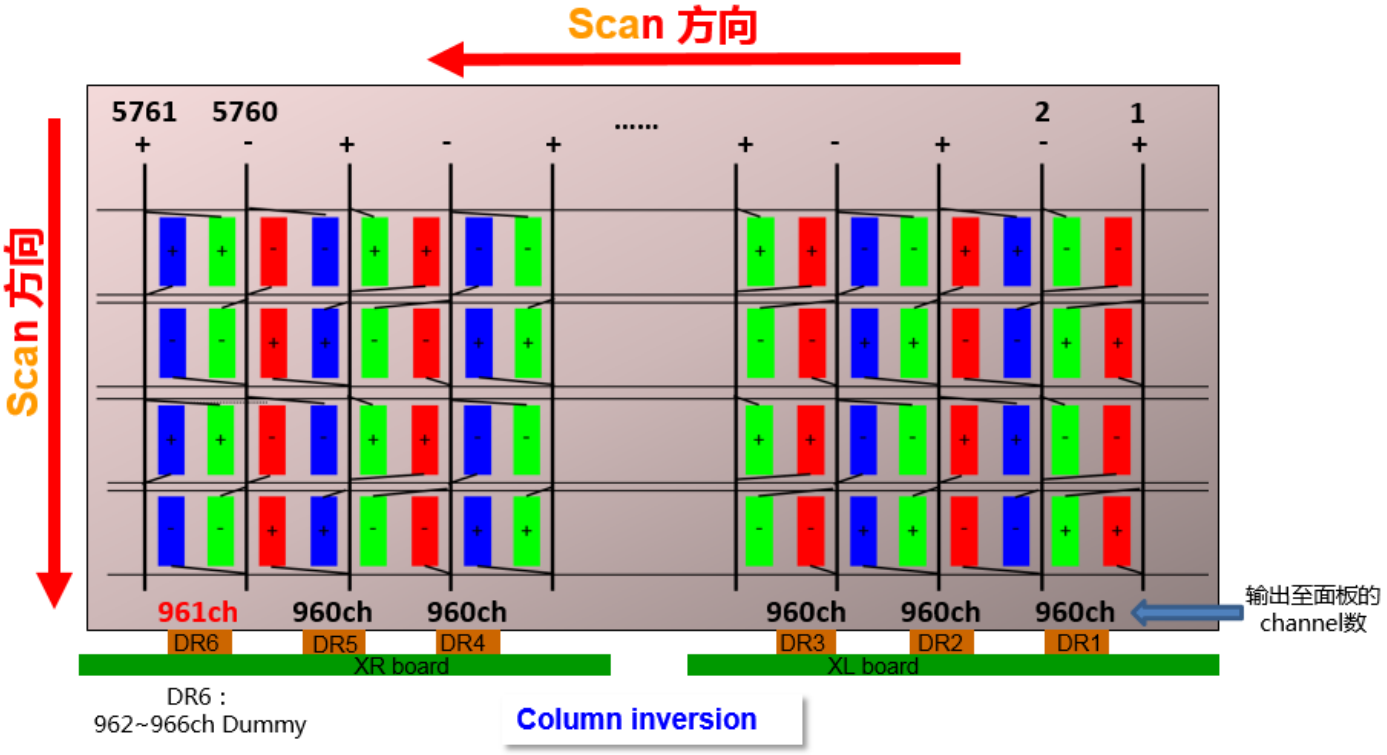


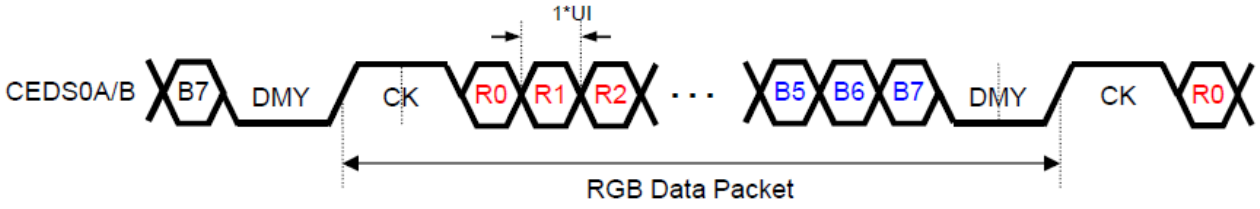
Fig. 6.3 Cell structure

6.3.2 Source driver data mapping

960CH, output direction: CH1→ CH960

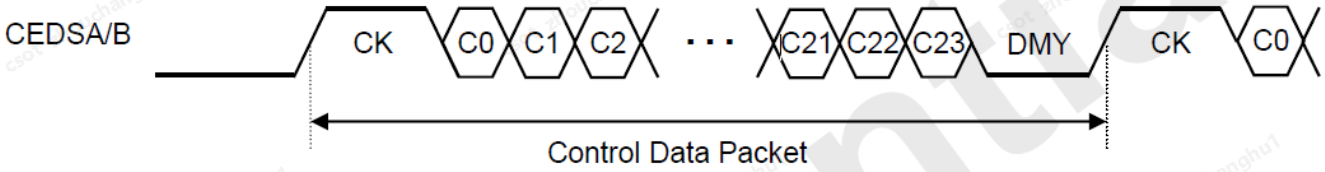
DR NO.	Data CH NO.				
DR1	1	2	3	……	960
DR2	961	962	963	……	1920
DR3	1921	1922	1923	……	2880
DR4	2881	2882	2883	……	3840
DR5	3841	3842	3843	……	4800
DR6	4801	4802	4803	……	5761

Table 6.3 Driver data output number



Bit	Name	Description
0, 1	CK	Indicates a rising edge of the embedded clock. (Always “H”)
2 ~ 25	-	RGB data are transmitted. MSB is transmitted at first. 2 ~ 9 : R0 ~ R7, 10 ~ 17 : G0 ~ G7, 18 ~ 25 : B0 ~ B7
26, 27	DMY	Dummy (Always “L”)

Fig. 6.4 input data mapping



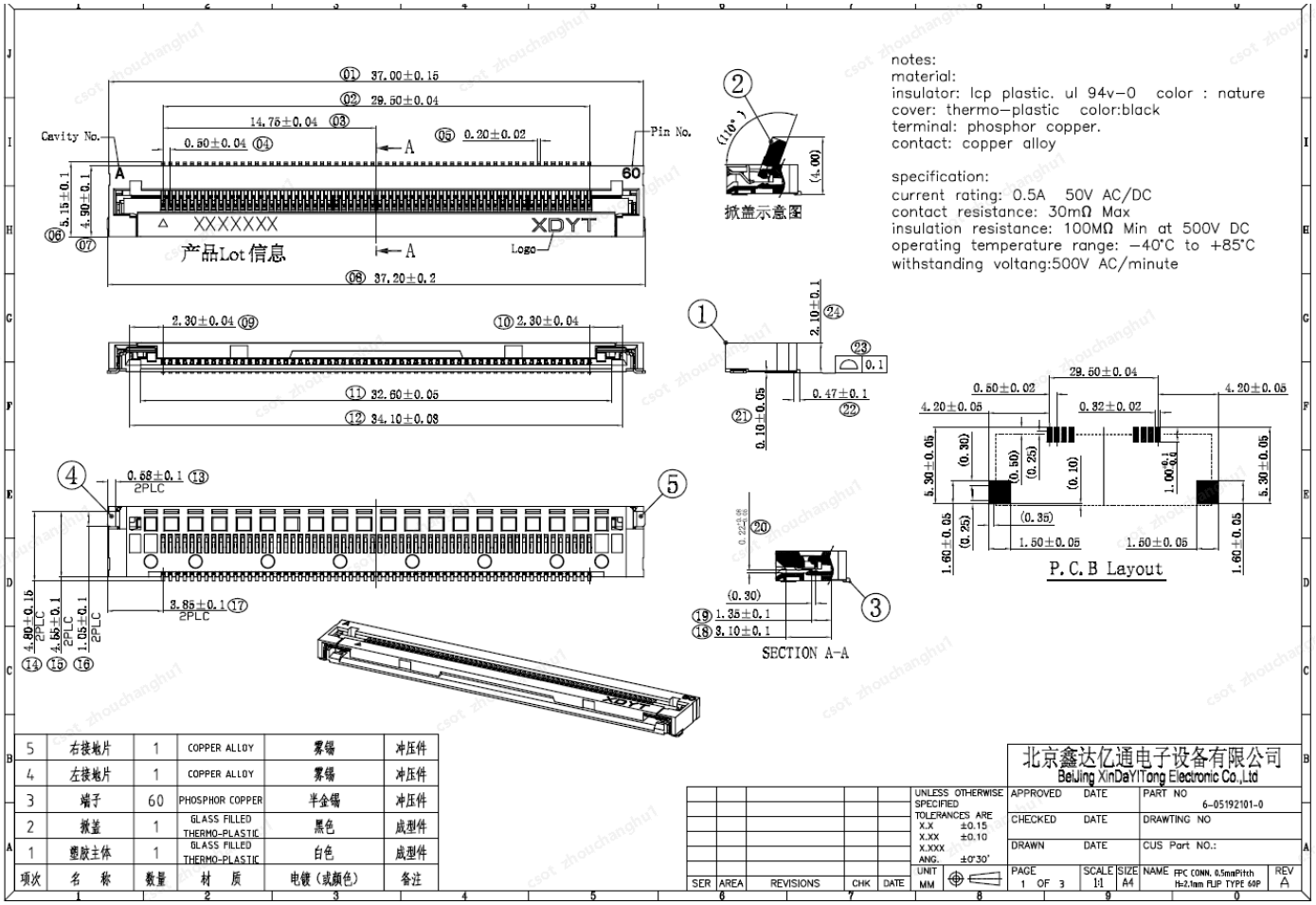
Bit	Name	Description
0, 1	CK	Indicates a rising edge of the embedded clock. (Always “H”)
2 ~ 25	-	Control packet data is transmitted. CTRS / CTR1 / CTR2 (CTR2 is available only when PKT_SEL = ‘H’) Please refer to “ 6. Control Data Packet Descriptions”
26, 27	DMY	Indicates a falling edge of the embedded clock. (Always “L”)

Fig. 6.5 Configuration mapping

Output	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	CH9	CH10	CH11	CH12
Order	1st data	2nd data	3rd data	4th data	5th data	6th data	7th data	8th data	9th data	10th data	11th data	12th data
Data	R1[0~7]	G1[0~7]	B1[0~7]	R2[0~7]	G2[0~7]	B2[0~7]	R3[0~7]	G3[0~7]	B3[0~7]	R4[0~7]	G4[0~7]	B4[0~7]
Output	CH949	CH950	CH951	CH952	CH953	CH954	CH955	CH956	CH957	CH958	CH959	CH960
Order	949th data	950th data	951th data	952th data	953th data	954th data	955th data	956th data	957th data	958th data	959th data	960th data
Data	R317[0~7]	G317[0~7]	B317[0~7]	R318[0~7]	G318[0~7]	B318[0~7]	R319[0~7]	G319[0~7]	B319[0~7]	R320[0~7]	G320[0~7]	B320[0~7]

Table 6.6 Each Driver data mapping

6.4 Input Connector& FFC Drawing

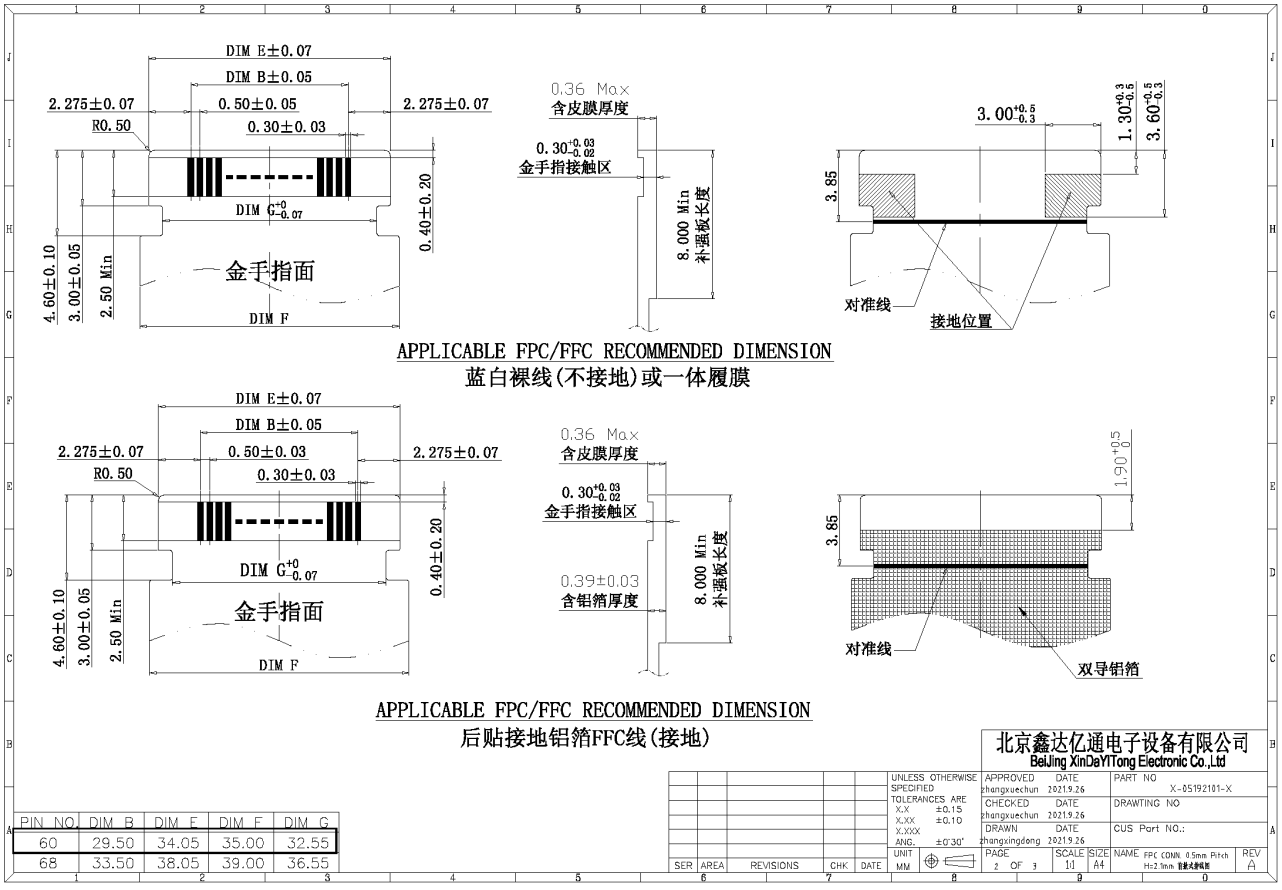


项次	名 称	数量	材 质	电镀（或颜色）	备注
5	右接地片	1	COPPER ALLOY	雾锡	冲压件
4	左接地片	1	COPPER ALLOY	雾锡	冲压件
3	端子	60	PHOSPHOR COPPER	半金锡	冲压件
2	掀盖	1	GLASS FILLED THERMO-PLASTIC	黑色	成型件
1	塑胶主体	1	GLASS FILLED THERMO-PLASTIC	白色	成型件

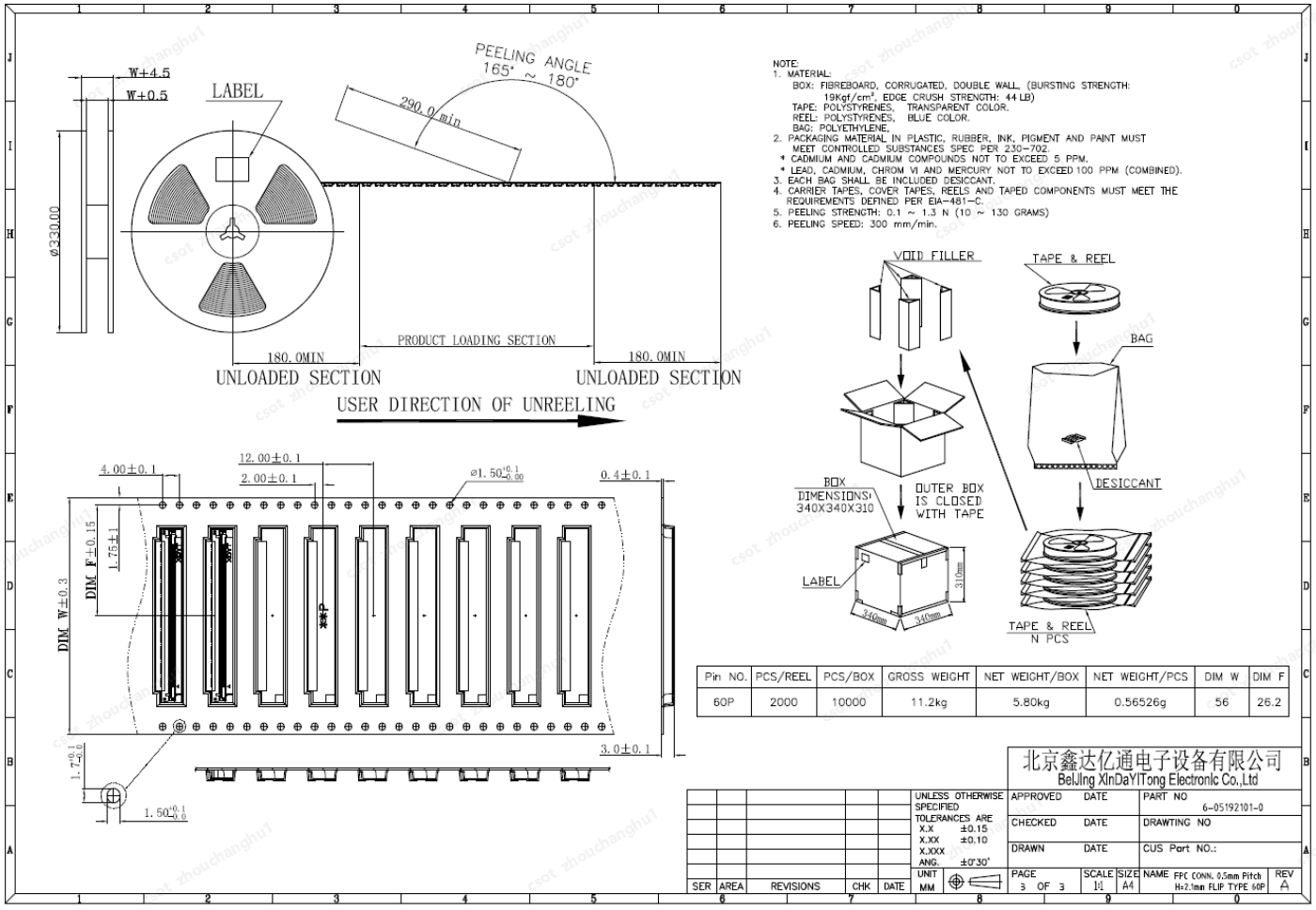
北京鑫达亿通电子设备有限公司
BeiJing XinDaYITong Electronic Co.,Ltd

UNLESS OTHERWISE SPECIFIED TOLERANCES ARE X.X ±0.15, X.XX ±0.10, X.XXX, ANG. ±0°30'	APPROVED DATE	PART NO 6-05192101-0	
	CHECKED DATE	DRAWTING NO	
	DRAWN DATE	CUS Part NO.:	
UNIT MM	PAGE 1 OF 3	SCALE 1:1	SIZE A4
NAME FPC CONN. 0.5mmPitch H=2.1mm FLIP TYPE 60P			REV A

SER | AREA | REVISIONS | CHK | DATE



PIN NO.	DIM B	DIM E	DIM F	DIM G
60	29.50	34.05	35.00	32.55
68	33.50	38.05	39.00	36.55



Pin NO.	PCS/REEL	PCS/BOX	GROSS WEIGHT	NET WEIGHT/BOX	NET WEIGHT/PCS	DIM W	DIM F
60P	2000	10000	11.2kg	5.80kg	0.56526g	56	26.2

北京鑫达亿通电子设备有限公司
BeiJing XinDaYITong Electronic Co.,Ltd

SER	AREA	REVISIONS	CHK	DATE

UNLESS OTHERWISE SPECIFIED TOLERANCES ARE X.X ±0.15 X.XX ±0.10 X.XXX ANG. ±0°30'

UNIT MM

APPROVED	DATE	PART NO
		6-05192101-0
CHECKED	DATE	DRAWTING NO
DRAWN	DATE	CUS Part NO.:

PAGE 3 OF 3 | SCALE 1/1 | SIZE A4 | NAME FPC CONN, 0.5mm Pitch H=2.1mm FLIP TYPE 60P | REV A

7. Optical Characteristics

7.1 Measurement Conditions

The table below is the test condition of optical measurement.

Item	Symbol	Value	Unit
Ambient Temperature	T_A	25±2	ºC
Ambient Humidity	H_A	50±10	%RH
Driving Signal	Refer to the typical value in Chapter 3: Electrical Specification		
Vertical Refresh Rate	F_R	60	Hz

To avoid abrupt temperature change during optical measurement, it's suggested to warm up the LCD module more than 60 minutes after lighting the backlight and in the windless environment.

To measure the LCD module, it is suggested to set up the standard measurement system as Fig. 7.1. The measuring area S should contain at least 500 pixels of the LCD module as illustrated in Fig.7.2(A means the area allocated to one pixel).In this model, for example, the minimum measuring distance Z is 370mm when θ is 2 degree. Hence, 500mm is the typical measuring distance. This measuring condition is referred to 301-2H of VESA FPDM 2.0 about viewing distance, angle, and angular field of view definition.

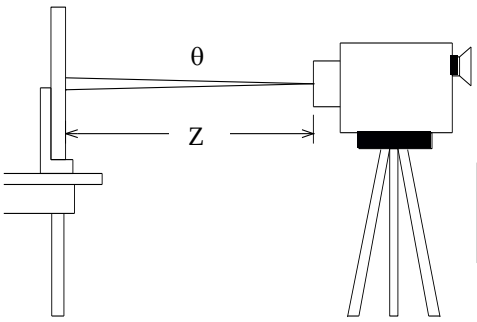


Fig. 7.1 The standard set-up system of measurement

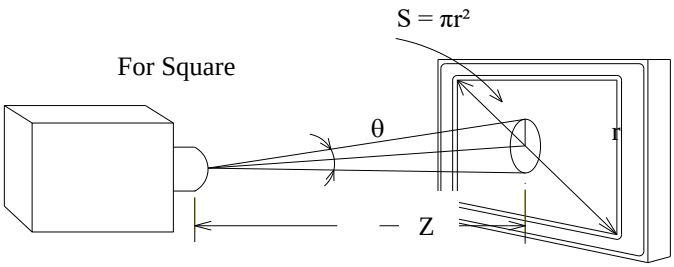


Fig. 7.2 The area S contains at least 500 pixels to be measured

$$N = \frac{S}{A} \geqslant 500\text{pixels}$$

N means the actual number of the pixels in the area S.

7.2 Optical Specifications

The table below of optical characteristics is measured by MINOLTA CS2000, MINOLTA CA310, ELDIM OPTIScope-SAand ELDIM EZContrast in dark room.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Static Contrast Ratio		CR	θH=0°, θV=0° Normal direction at center point CSOT's module: ST4251D02-3	3000	4000	-	-	(1)(2)
Response Time		T_L		-	6.5	12	ms	(3)OPTIScope-SA
Center Transmittance		T%		3.87%	4.3%			(2) (4)
Gamma		-		2.0	2.2	2.4	-	Base on 50~128 gray, CSOT will continuously monitor
Crosstalk		CT		-	-	4%	-	(2) (5)
Color Chromaticity (CIE1931)	Red	R_X		Typ. -0.02	0.639	Typ. +0.02	-	(2) (6)
		R_Y			0.336		-	
	Green	G_X			0.296		-	
		G_Y			0.616		-	
	Blue	B_X			0.150		-	
		B_Y			0.063		-	
	White	W_X			0.272		-	
		W_Y			0.311		-	
	Color Gamut	CG		68	72%	-	%NTSC	(2) (6)
Viewing Angle	Horizontal	θ_{H+}	CR≥ 10	-	89	-	Deg.	(7)
		θ_{H-}		-	89	-		
	Vertical	θ_{V+}		-	89	-		
		θ_{V-}		-	89	-		
Gray Scale		0	(Grayn-Gray0)/ (Gray255-Gray0)*100%		0.00%			
		1			0.00%			
		31			1.12%			
		63			4.76%			
		127			21.03%			
		191			51.20%			
		223			72.65%			
		254			99.08%			
		255			100.00%			

Note:

(1) Definition of static contrast ratio (CR):

It's necessary to switch off all the dynamic and dimming function when measuring the static contrast ratio.

$$\text{Static Contrast Ratio (CR)} = \frac{\text{CR-W}}{\text{CR-D}}$$

CR-W is the luminance measured by LMD (light-measuring device) at the center point of the LCD module with full-screen displaying white. The standard setup of measurement is illustrated in Fig. 6.3; CR-D is the luminance measured by LMD at the center point of the LCD module with full-screen displaying black.

(2) The LMD in the item could be a spectroradiometer such as (KONICA MINOLTA) CS2000, CS1000, (TOPCON) SR-UL2 or the same level spectroradiometer. Other display color analyzer (KONICA MINOLTA) CA210, CA310 or (TOPCON) BM-7 could be involved after being calibrated with a spectroradiometer on each stage of a product.

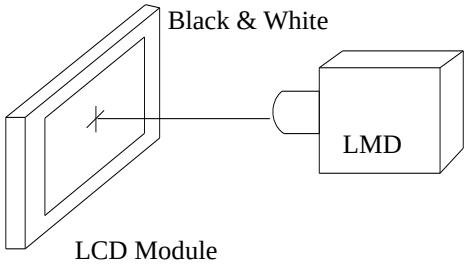


Fig. 7.3 The standard setup of CR measurement

(3) Response time T_L is defined as the average transition time in the response time matrix. The table below is the response time matrix in which each element $t_{X\ to\ Y}$ is the transition time from gray level X to Y. X and Y are two different gray level samong0%, 25%, 50%, 75%, and 100% gray level. The transition time $t_{X\ to\ Y}$ is defined as the time taken from 10% to 90% of the luminance difference between X and Y (X<Y) as illustrated in Fig6.4. When X>Y, the definition of $t_{X\ to\ Y}$ is the time taken from 90% to 10% of the luminance difference between X and Y. The response time is optimized on refresh rate F_R=60 Hz.

Measured Transition Time		Luminance Ratio of Previous Frame				
		0%	25%	50%	75%	100%
Gray level of Current Frame	0%		$t_{25\%\ to\ 0\%}$	$t_{50\%\ to\ 0\%}$	$t_{75\%\ to\ 0\%}$	$t_{100\%\ to\ 0\%}$
	25%	$t_{0\%\ to\ 25\%}$		$t_{50\%\ to\ 25\%}$	$t_{75\%\ to\ 25\%}$	$t_{100\%\ to\ 25\%}$
	50%	$t_{0\%\ to\ 50\%}$	$t_{25\%\ to\ 50\%}$		$t_{75\%\ to\ 50\%}$	$t_{100\%\ to\ 50\%}$
	75%	$t_{0\%\ to\ 75\%}$	$t_{25\%\ to\ 75\%}$	$t_{50\%\ to\ 75\%}$		$t_{100\%\ to\ 75\%}$
	100%	$t_{0\%\ to\ 100\%}$	$t_{25\%\ to\ 100\%}$	$t_{50\%\ to\ 100\%}$	$t_{75\%\ to\ 100\%}$	

$t_{X\ to\ Y}$ means the transition time from luminance ratio X to Y.

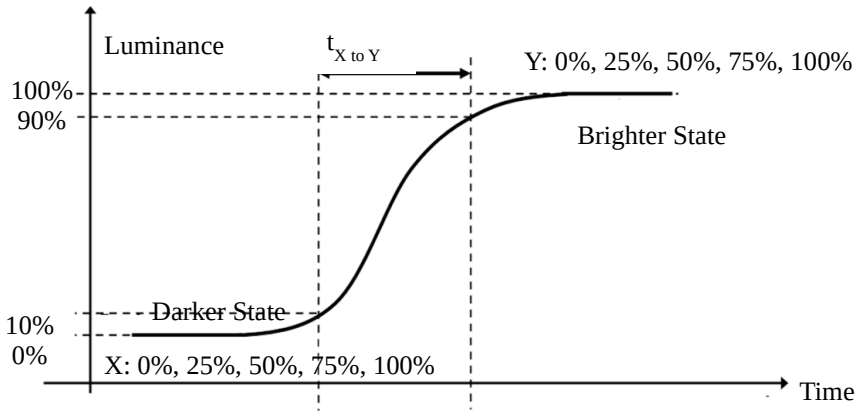


Fig. 7.4 The definition of $t_{X\ to\ Y}$

All the transition time is measured at the center point of the LCD module by ELDIM OPTI Scope-SA.

(4) Definition of center Transmittance (T %):

The transmittance is measured with full white pattern (Gray 255)

$$\text{Transmittance (T \%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}}$$

(5) Definition of the 2D mode crosstalk (CT-2D):

YA = Luminance of measured location without gray level 255 pattern (cd/m^2)

YB = Luminance of measured location with gray level 255 pattern (cd/m^2)

Definition of the 2D mode crosstalk: $CT\text{-}2D = \frac{YB\text{-}YA}{YA}$

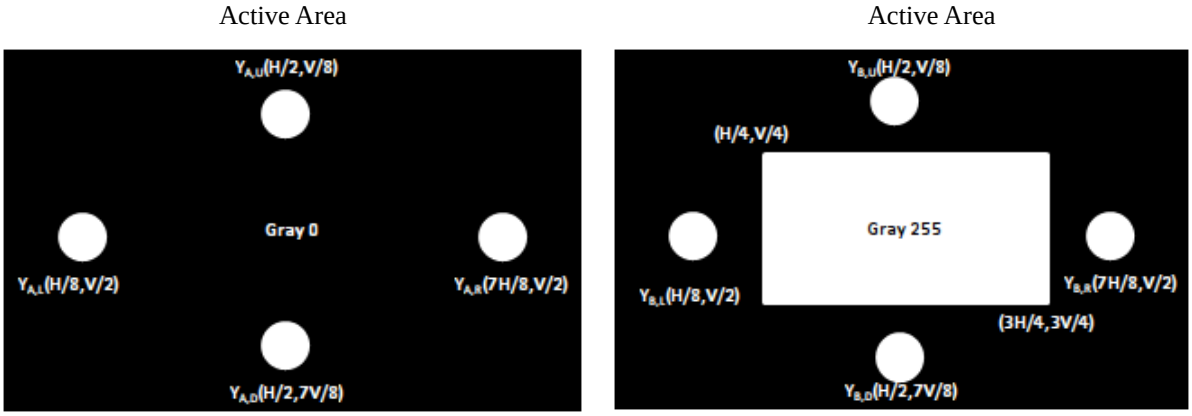


Fig. 7.5 The definition of 2D mode crosstalk

(6) Definition of color chromaticity:

Each chromaticity coordinates (x, y) are measured in CIE1931 color space when full-screen displaying primary color R, G, B and white. The color gamut is defined as the fraction in percent of the area of the triangle bounded by R, G, B coordinates and the area is defined by NTSC 1953 color standard in the CIE color space. Chromaticity coordinates are measured by CS2000 and the standard setup of measurement is shown in Fig. 7.6

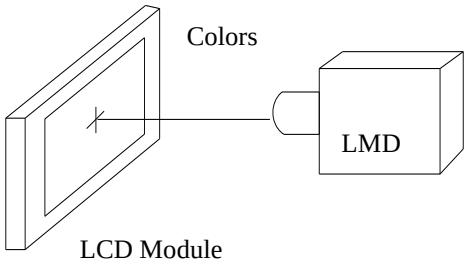


Fig. 7.6 The standard setup of color chromaticity measurement

(7) Definition of viewing angle coordinate system (θ_H,θ_V):

The contrast ratio is measured at the center point of the LCD module. The viewing angles are defined at the angle that the contrast ratio is larger than 10 at four directions relative to the perpendicular direction of the LCD module (two vertical angles: up θ_{V+} and downθ_{V-}; and two horizontal angles: right θ_{H+} and leftθ_{H-}) as illustrated in Fig. 7.7. The contrast ratio is measured by ELDIM EZ Contrast.

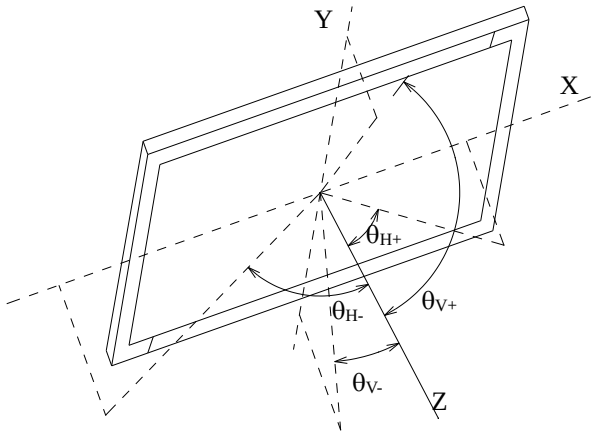
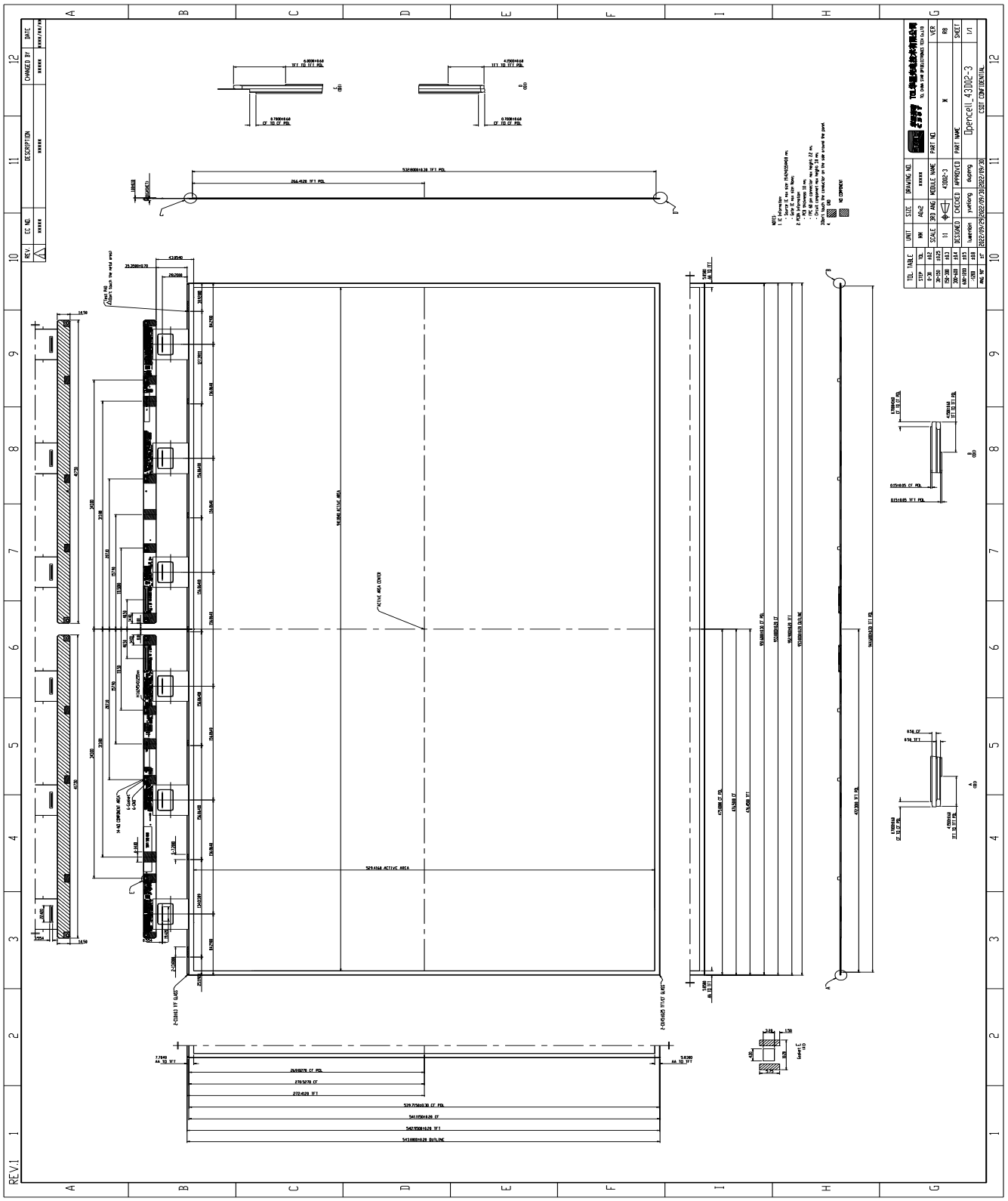


Fig. 7.7 Viewing angle coordination system

8. Mechanical Characteristics

8.1 Mechanical Specification

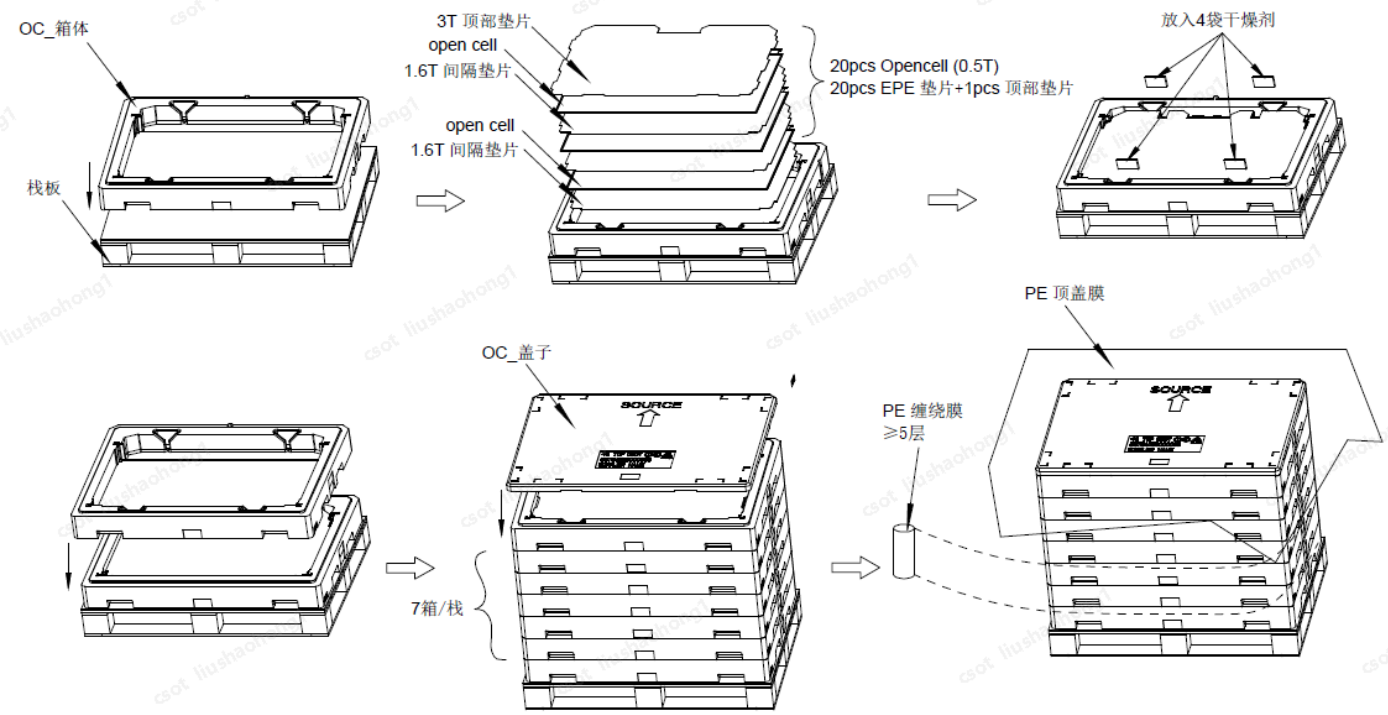


8.2 Packing

8.2.1 Packing Specifications

Item	Specification		
	Quantity	Dimension (mm)	Weight (kg)
Packing Box	20pcs/box	1130.00(L) x 830.00(W) x125.00 (H)	Net Weight: 32.6 Gross Weight: 35.8
Pallet	1	1150.00 (L) x 850.00 (W) x 130.00 (H)	Net Weight: 13
Stack Layer	7		
Boxes per Pallet	7		
Pallet after Packing	140 pcs/pallet	1150.00 (L) x 850.00 (W) x975.00(H)	Gross Weight: 265
Pallet Stack Layer	2 layers/Warehouse, 2 layer/40GP, 2 layer/40HQ.		

8.2.2 Packing Method



9. Definition of Labels

9.1 Open Cell Label

XXXXXXXXXXXXXXXXXXXXXXXX ST4251D02-3 Ver. X.X

- Model Version Code
- Model Name
- Week Code
- Serial Number

Serial Number: XXXXXXXXXXXXXXXXXXX

- CSOT Internal Use
- Panel ID

Week Code: XXXX

- Week
- Year

Year: 2010 =10, 2011 = 11 …2020= 20, 2021= 21…

Week: 01, 02, 03 …

Model Name: ST4251D02-3

Ver.X.X: Version, for example: 0.1, 0.2, 1.1, 1.2… 2.1, 2.2 …

9.2 Carton Label

For RoHS compliant products, CSOT will add RoHS for identification.

Serial Number: XXXXXXXXXXXXXXXXXXX

- CSOT Internal Use
- Year, Month, Date
- Model Version Code
- CSOT Internal Use

Manufactured Date:

Year: 2010 =10, 2011 = 11…2020= 20, 2021= 21…

Month: 1~9, A~C, for Jan. ~ Dec.

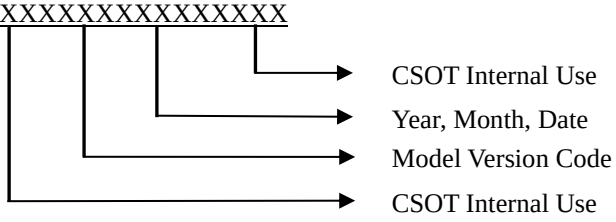
Date: 01~31, for 1st to 31st

Model Version Code: Version of product, for example: 01, 02, 11, 12…

9.3 Pallet Label

Model Name: ST4251D02-3

Serial Number: XXXXXXXXXXXXXXXXXX



10. Precautions

10.1 Assembly and Handling Precautions

(1) The device listed in the product specification sheets was designed and manufactured for TV application only.

(2) Do not apply rough force such as bending or twisting to the open cell during assembly.

(3) It is recommended to assemble or install an open cell into the user's system in clean working areas. The dust and oil may cause electrical shorter damage the polarizer.

(4) Any attachment on polarizer of open-cell，such as tape，is forbidden and not recommend，especially under the hightemperature and high humidity environment.

(5) Do not apply pressure or impulse to the open cell to prevent the damage to the open cell.

(6) Always follow the correct power-on sequence. This can prevent the damage and latch-up to the LSI chips.

(7) Do not plug in or pull out the interface connector while the open cell is in operation.

(8) Use soft dry cloth without chemicals for cleaning because the surface of polarizer is very soft and easily be scratched.

(9) Moisture can easily penetrate into the open cell and may cause the damage during operation.

(10) High temperature or humidity may deteriorate the performance of the open cell. Please store open cell in the specified storage conditions.

(11) When ambient temperature is lower than 10ºC, the display quality might be deteriorated. For example, the response time will become slow.

(12) Since a panel is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly. Panel ground path should be connected to metal ground.

(13) Panel should be protected from the static electricity. If not, it causes IC damage.

(14) Do not pull or fold the source D-IC which connect the source PCB and the panel.

(15) Surface temperature of the Component on PCB should be controlled under 100℃ (D-IC : 120℃) with TV Set status. If not, problems such as IC damage or decrease of lifetime could occur.

(16) POL Protective film peeling Precautions：peeling from source side to the opposite; peeling speed：≤30m/min

10.2 Safety Precautions

(1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(2) After the open cell end of life, it is not harmful in case of normal operation and storage.

10.3 Reliability test

The reliability test items and conditions shown as below：

Item	Test condition
HTHHO	60℃ 90%RH，240hrs
HTO	50℃，240hrs
LTO	-15℃，240hrs
HT-Start	60℃ (Power off 2hr/on 10min)/Cyc
LT-Start	-15℃ ，(Power On 10s/off 10s)/Cyc

HTHHS	60℃ 90%RH，240hrs
Thermal Shock	（-20℃，0.5hr → 60℃，0.5hr）/cycle，100cycles
LTS	-20℃，240hrs
Packing Vibration	1~200Hz；1.3Grms X, Y, Z three axis (30min /axis）

Note：This Test Condition is based on CSOT Module，and before and after Reliability test，LCM should be operated with normal function

10.4 International Standards

(1) CSOT can meet the RoHS standard.

(2) RoHS,Directive of the European Parliament and of the Council on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment, 2011/65/EU, June 2011 (RoHS Directive) and 2015/863/EU, June 2015 (addition of four phthalates).

(3) REACH,Regulation(EU) NO 1907/2006 of the European Parliament and of the Council of 18 December 2006 concerning the Regulation,Evaluation,Authorization and Restriction of Chemicals.