☐ Tentative Specification
■ Preliminary Specification
☐ Approval Specification

MODEL NO.: VA00DK1

SUFFIX: QS1

Revision :
Customer :

APPROVED BY SIGNATURE

Name / Title
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Chih-Fan Ting	Chia-Wen Chen

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver. 1.0	5/19,2016	All	All	The preliminary specification was been released.

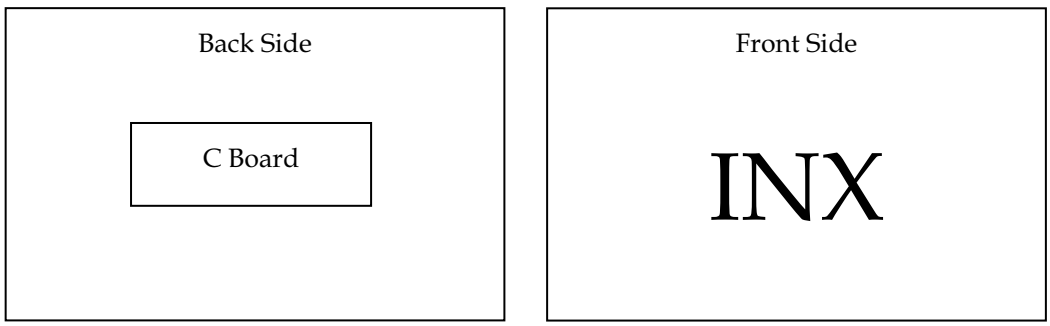
1. GENERAL DESCRIPTION

1.1 OVERVIEW

VA00DK1-QS1 is a 99.5″ TFT Liquid Crystal Display product with driver ICs and 16 lane V by One interface. This product supports 3840 x 2160 QHDTV format and can display true 1.07G colors (8-bit+FRC). The backlight unit is not built in.

1.2 FEATURES

CHARACTERISTICS ITEMS	SPECIFICATIONS
Pixels [lines]	3840 × 2160
Active Area [mm]	2203.2(H) x 1239.3(V)
Sub-Pixel Pitch [mm]	0.19125(H) x 0.5735(V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	11240g
Physical Size [mm]	2220.6 (W) x 1257.3(H) x 1.75(D) Typ
Display Mode	Transmissive mode / Normally black
Contrast Ratio	(4000:1) Typ. (Typical value measured at INX's module)
Glass thickness (Array / CF) [mm]	0.7 / 0.7
Viewing Angle (CR>10) (VA Model)	+89/-89 (H),+89/-89(V) Typ. (Typical value measured by INX's module)
Color Chromaticity	R=(0.672, 0.319) G=(0.264, 0.615) B=(0.136, 0.094) W=(0.295, 0.345) * Please refer to "color chromaticity" in 7.2
Cell Transparency [%]	(4.9%) Typ. Please refer to "Transmittance" in 7.2
Polarizer Surface Treatment	AGLR, 3H
Rotation Function	Unachievable
Display Orientation	Signal input with "INX"
RoHs Compliance	
This Open Cell is using FPC to link X-Board , Please refer mechanical drawing in Chapter 11	

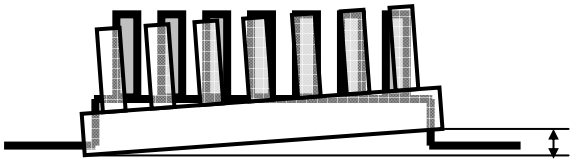


1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight	10678	11240	11802	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within ± 0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position



2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1), (3)
Operating Ambient Temperature	T_{OP}	0	50	ºC	(1), (2), (3)

Note (1) Temperature and relative humidity range is shown in the figure below.

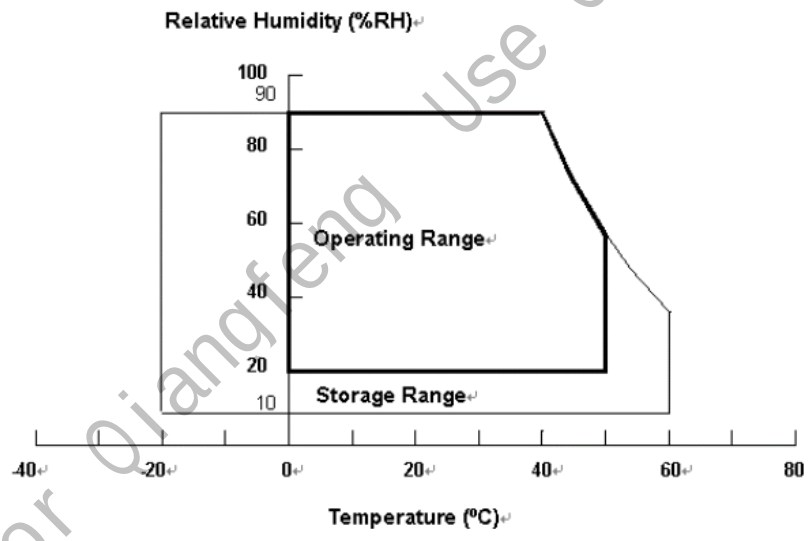
(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max.

(c) No condensation.

Note (2) Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) The rating of environment is base on LCD module. Leave LCD cell alone, this environment condition can't be guaranteed. Except LCD cell, the customer has to consider the ability of other parts of LCD module and LCD module process.



2.2 ABSOLUTE RATINGS OF ENVIRONMENT (OPEN CELL)

Recommended Storage Condition: With shipping package.

Recommended Storage temperature range: 25±5 ℃

Recommended Storage humidity range: 50±10%RH

Recommended Shelf life: a month

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	
Component thermal	---	---	Tj(max.)	℃	(2)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) It is important and necessary to follow the Thermal Application Note, otherwise it may lead to abnormal display or component damage. INX thermal application note would be provided by INX in the design-in stage.

3. ELECTRICAL CHARACTERISTICS

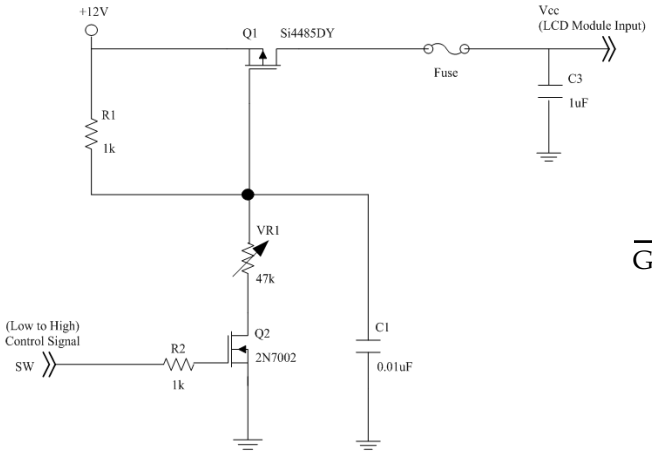
3.1 TFT LCD Module

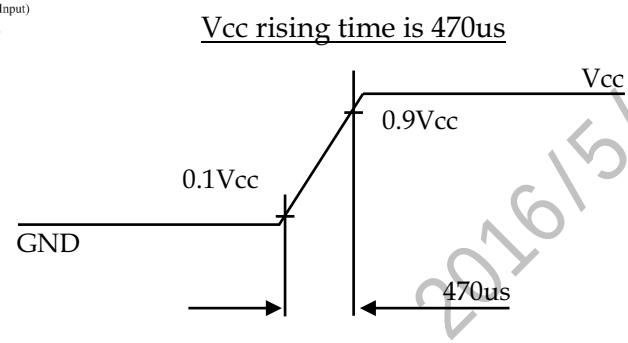
(Ta = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	—	—	(9.62)	A	(2)
Power consumption	White Pattern	P_T	—	(25.82)	(28.4)	W	(3)
	Black Pattern	P_T	—	(25.49)	(28.04)		
	Heavy Loading pattern 2W2B (by cell and platform)	P_T	—	(70.92)	(78.01)		
Power Supply Current	White Pattern	P_T	—	(2.24)	(2.7)	A	
	Black Pattern	P_T	—	(2.21)	(2.66)		
	Heavy Loading pattern 2W2B (by cell and platform)	P_T	—	(6.12)	(7.42)		
V-by-One HS	Differential Input High Threshold Voltage	V_{LVTH}		—	+50	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	-50	—	—	mV	
	Differential Input Resistor	R_{RIN}	80	100	120	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges. The ripple voltage should be controlled under 10% of Vcc (Typ.).

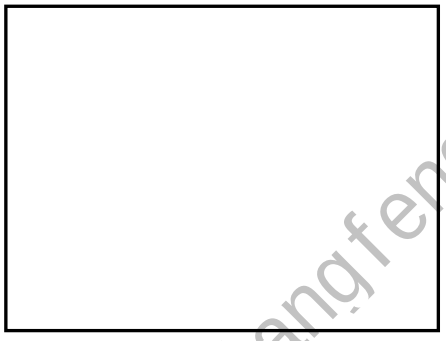
Note (2) Measurement condition :





Note (3) The specified power consumption and power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 °C, f_v = 120 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

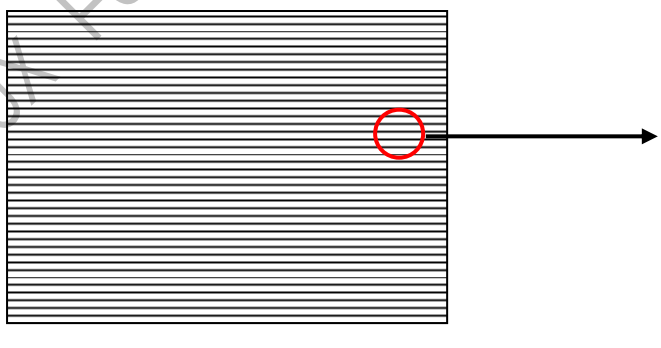


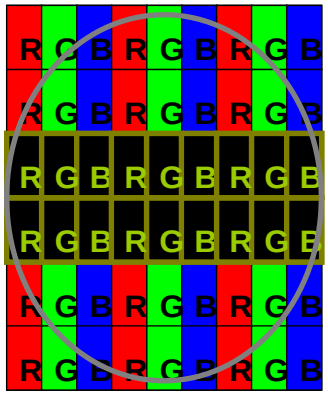
Active Area

b. Black Pattern

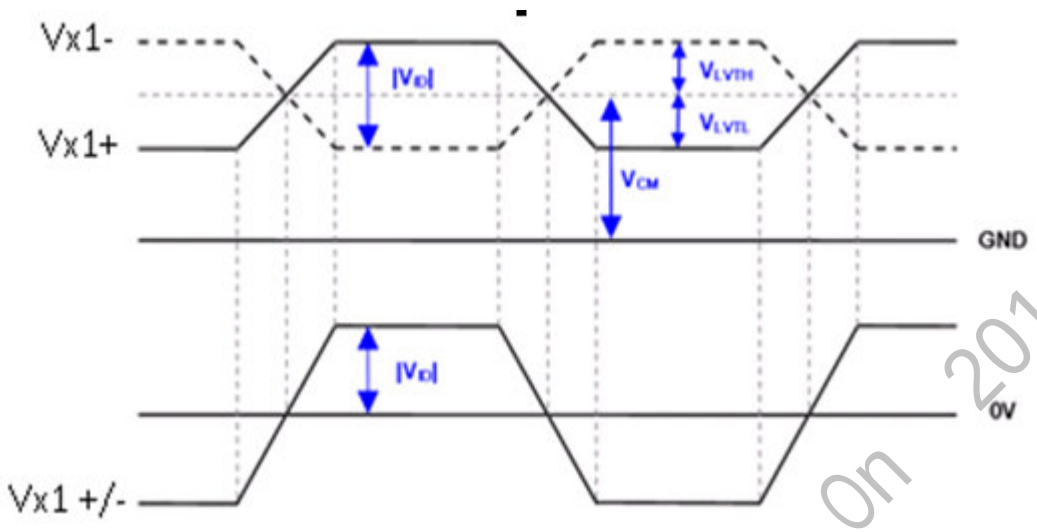
Active Area

c. Heavy Loading pattern





Note (4) The V-by-One input characteristics are as follows:



4. INPUT TERMINAL PIN ASSIGNMENT

4.1 TFT LCD OPEN CELL

CNV1 Connector Pin Assignment Mating connector: FI-RE51S-HF (JAE)

Pin	Name	Description	Note
1	N.C.	No Connection	(10)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	N.C.	No Connection	
8	N.C.	No Connection	
9	N.C.	No Connection	(15)
10	GND	Ground	
11	GND	Ground	
12	GND	Ground	
13	GND	Ground	
14	GND	Ground	
15	L/R_O	Output signal for Glasses Left Right signal,	(5)
16	L/R_I	Input signal for Left/Right synchronous signal.	(3) (7)
17	2D/3D	2D/3D Enable	(2) (7)
18	SDA	I2C Data signal	(6)
19	SCL	I2C Clock signal	(6)
20	WP	Write Protection (0V~0.7V/Open→Disable, 2.7V~3.3V→Enable) (for Auto-Vcom)	(13)
21	N.C.	No Connection	(10)
22	N.C.	No Connection	(14)
23	TST_AGE	TST_AGE Enable(High level is enable aging mode)	(7)
24	N.C.	No Connection	(10)
25	HTPDN	Hot plug detect output, Open drain.	
26	LOCKN	Lock detect output, Open drain.	
27	GND	Ground	
28	RX0N	1ST Pixel Negative VbyOne differential data input in area A. Lan 0	(1)
29	RX0P	1ST Pixel Positive VbyOne differential data input in area A. Lan 0	
30	GND	Ground	
31	RX1N	2ND Pixel Negative VbyOne differential data input in area A. Lan 1	(1)
32	RX1P	2ND Pixel Positive VbyOne differential data input in area A. Lan 1	

33	GND	Ground	
34	RX2N	3RD Pixel Negative VbyOne differential data input in area A. Lan 2	(1)
35	RX2P	3RD Pixel Positive VbyOne differential data input in area A. Lan 2	
36	GND	Ground	
37	RX3N	4TH Pixel Negative VbyOne differential data input in area A. Lan 3	(1)
38	RX3P	4TH Pixel Positive VbyOne differential data input in area A. Lan 3	
39	GND	Ground	
40	RX4N	5TH Pixel Negative VbyOne differential data input in area A. Lan 4	(1)
41	RX4P	5TH Pixel Positive VbyOne differential data input in area A. Lan 4	
42	GND	Ground	
43	RX5N	6TH Pixel Negative VbyOne differential data input in area A. Lan 5	(1)
44	RX5P	6TH Pixel Positive VbyOne differential data input in area A. Lan 5	
45	GND	Ground	
46	RX6N	7TH Pixel Negative VbyOne differential data input in area A. Lan 6	(1)
47	RX6P	7TH Pixel Positive VbyOne differential data input in area A. Lan 6	
48	GND	Ground	
49	RX7N	8TH Pixel Negative VbyOne differential data input in area A. Lan 7	(1)
50	RX7P	8TH Pixel Positive VbyOne differential data input in area A. Lan 7	
51	GND	Ground	

CNV2 Connector pin assignment Mating connector: FI-RE41S-HF(JAE)

Pin	Name	Description	Note
1	GND	Ground	
2	RX8N	1ST Pixel Negative VbyOne differential data input in area B. Lan 8	(1)
3	RX8P	1ST Pixel Positive VbyOne differential data input in area B. Lan 8	
4	GND	Ground	
5	RX9N	2ND Pixel Negative VbyOne differential data input in area B. Lan 9	(1)
6	RX9P	2ND Pixel Positive VbyOne differential data input in area B. Lan 9	
7	GND	Ground	
8	RX10N	3RD Pixel Negative VbyOne differential data input in area B. Lan 10	(1)
9	RX10P	3RD Pixel Positive VbyOne differential data input in area B. Lan 10	
10	GND	Ground	
11	RX11N	4TH Pixel Negative VbyOne differential data input in area B. Lan 11	(1)

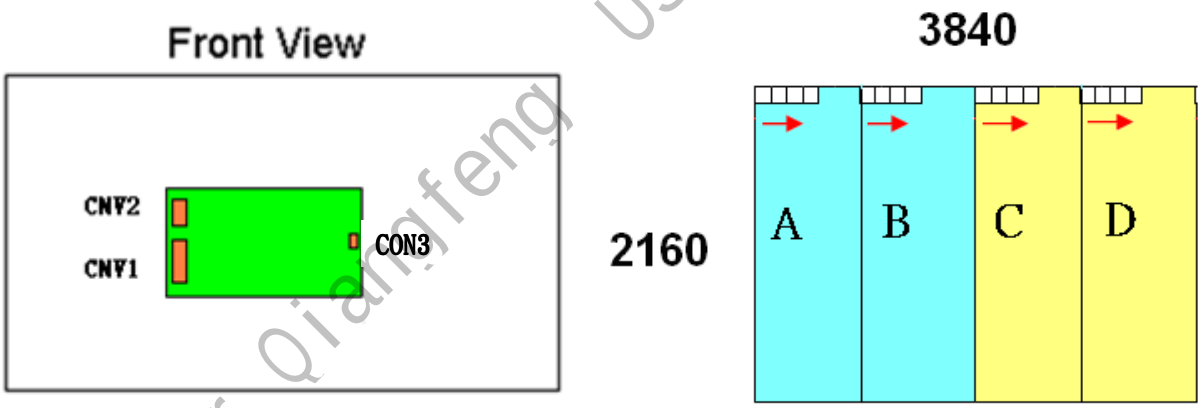
12	RX11P	4TH Pixel Positive VbyOne differential data input in area B. Lan 11	
13	GND	Ground	
14	RX12N	5TH Pixel Negative VbyOne differential data input in area B. Lan 12	(1)
15	RX12P	5TH Pixel Positive VbyOne differential data input in area B. Lan 12	
16	GND	Ground	
17	RX13N	6TH Pixel Negative VbyOne differential data input in area B. Lan 13	(1)
18	RX13P	6TH Pixel Positive VbyOne differential data input in area B. Lan 13	
19	GND	Ground	
20	RX14N	7TH Pixel Negative VbyOne differential data input in area B. Lan 14	(1)
21	RX14P	7TH Pixel Positive VbyOne differential data input in area B. Lan 14	
22	GND	Ground	
23	RX15N	8TH Pixel Negative VbyOne differential data input in area B. Lan 15	(1)
24	RX15P	8TH Pixel Positive VbyOne differential data input in area B. Lan 15	
25	GND	Ground	
26	SPI_ENA	Enable SPI BUS Switch A	(4)
27	SPIF_SO_I	SPI Data input (to T-con Flash DI)	
28	SPIF_SI_I	SPI Data output (to T-con Flash DO)	
29	N.C.	No Connection	(10)
30	VCA	Enable Flicker adjustment	
31	N.C.	No Connection	(14)
32	N.C.	No Connection	
33	N.C.	No Connection	
34	N.C.	No Connection	
35	SPI_ENB	Enable SPI BUS Switch B	(4)
36	SPIF_CK_I	SPI Clock signal	
37	SPIF_CSN_I	SPI enable signal	
38	N.C.	No Connection	(14)
39	N.C.	No Connection	(14)
40	N.C.	No Connection	(10)
41	N.C.	No Connection	(14)

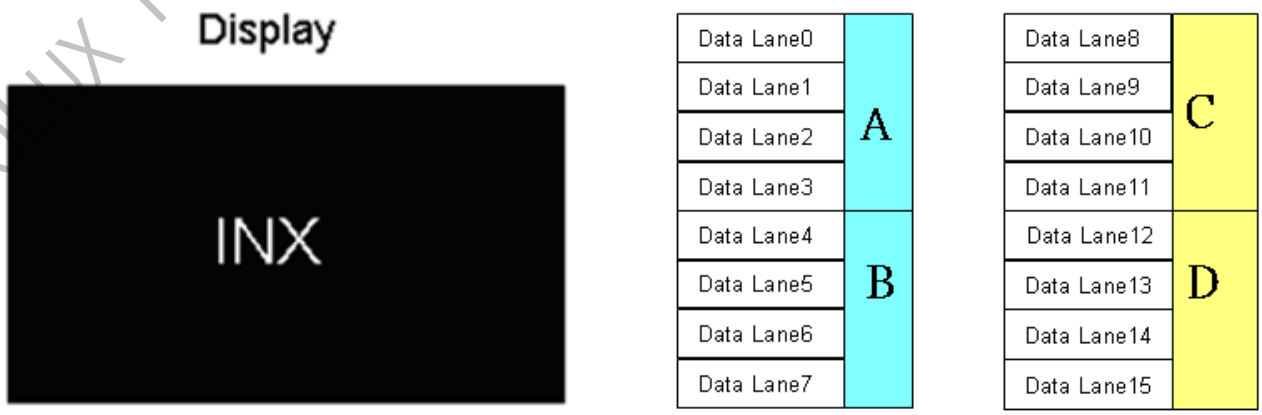
CON3 Connector Pin Assignment (SM05B-PASS-TBT(LF)(SN))

1	GND	Ground	
2	GND	Ground	
3	Vin	Power input (+12V)	(12)
4	Vin	Power input (+12V)	
5	Vin	Power input (+12V)	

Note (1) V-by-One® HS Data Mapping

Area	Lane	Data Stream
A	Lane 0	1, 5, 9, ..., 953, 957
	Lane 1	2, 6, 10, ..., 954, 958
	Lane 2	3, 7, 11, ..., 955, 959
	Lane 3	4, 8, 12, ..., 956, 960
B	Lane 4	961, 965, 969, ..., 1913, 1917
	Lane 5	962, 966, 970, ..., 1914, 1918
	Lane 6	963, 967, 971, ..., 1915, 1919
	Lane7	964, 968, 972, ..., 1916, 1920
C	Lane 8	1921, 1925, 1929, ..., 2873, 2877
	Lane 9	1922, 1926, 1930, ..., 2874, 2878
	Lane 10	1923, 1927, 1931, ..., 2875, 2879
	Lane 11	1924, 1928, 1932, ..., 2876, 2880
D	Lane12	2881, 2885, 2889, ..., 3833, 3837
	Lane 13	2882, 2886, 2890, ..., 3834, 3838
	Lane 14	2883, 2887, 2891, ..., 3835, 3839
	Lane 15	2884, 2888, 2892, ..., 3836, 3840





Note (2) 2D/3D mode selection.

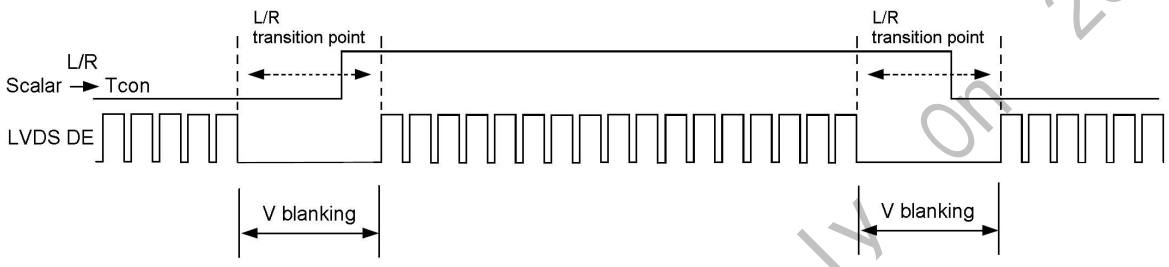
L= Connect to GND or Open, H=Connect to +3.3V

2D/3D	Note
L or Open	2D Mode
H	3D Mode

Note (3) Input signal for Left Right eye frame synchronous

V_{IL}=0~0.8 V, V_{IH}=2.0~3.3 V

L/R	Note
L	Right synchronous signal
H	Left synchronous signal



Note (4) SPI_ENA & SPI_ENB enable selection. (Default: Disable)

L= Connect to GND or Open(0V~0.7V), H=Connect to +3.3V (2.7V~3.3V)

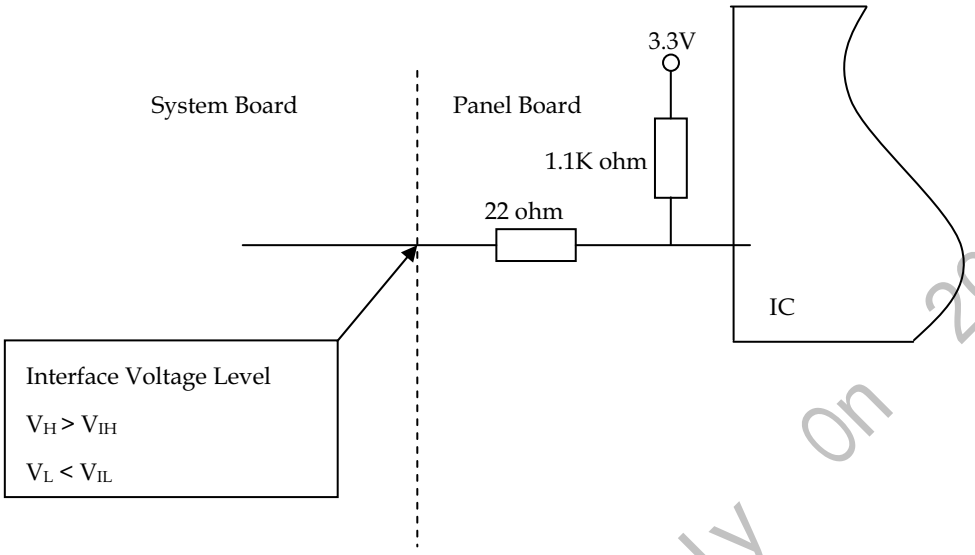
SPI_ENA & SPI_ENB	Note
L or Open	Disable
H	Enable

Note (5) The definition of L/R_O signal as follows

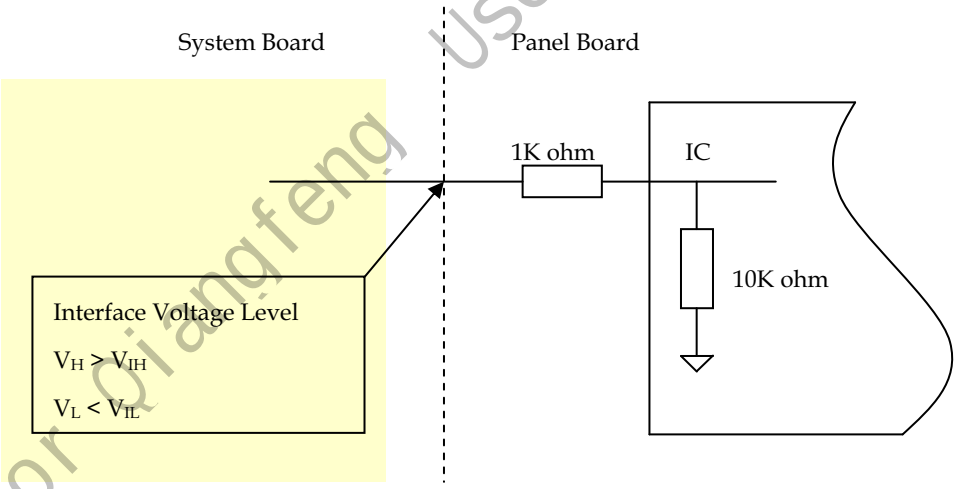
L= 0V , H= +3.3V

L/R_O	Note
L	Right glass turn on
H	Left glass turn on

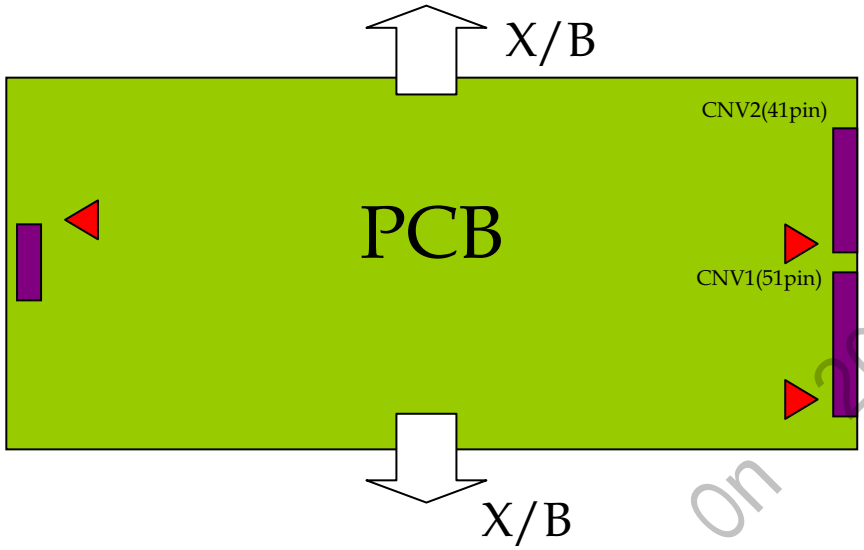
Note (6) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement which including Panel board loading as below.



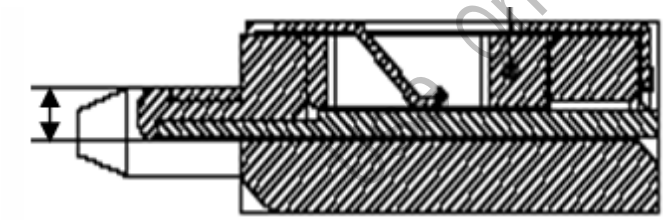
Note (7) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement which including Panel board loading as below.



Note (8) V-by-One HS connector pin order defined as follows



Note (9) V-by-One connector mating dimension range request is 0.93mm~1.0mm as below



Note (10) Reserved for internal use. Please leave it open.

Note (11) Local dimming table select for customer use.

Note (12) (Optional) Power input (+12V), Please check the current rating of FFC cable to meet the power consumption requirement.

Note (13) Digital auto VCOM adjust control pin.

WP	Mode
L(default)	Internal week pull-low
H	Auto-VCOM adjust mode.

Note (14) Not connected in Tcon board

Note (15) Not connected in Tcon board. Please leave it open to avoid 12V-GND short, too.

4.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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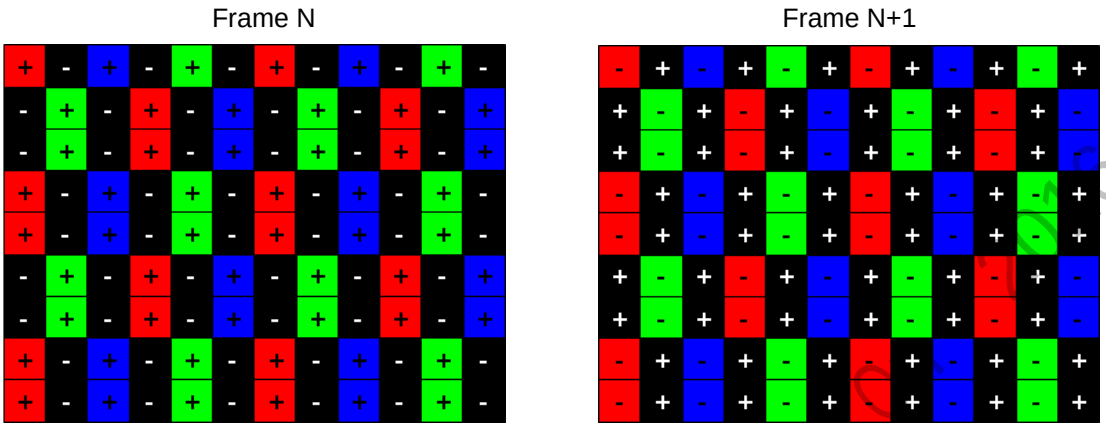
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage，1: High Level Voltage

4.3 FLICKER (Vcom) ADJUSTMENT

(1) Adjustment Pattern:

Column-inversion pattern was shown as below. If customer need below pattern, please directly contact with Account FAE.



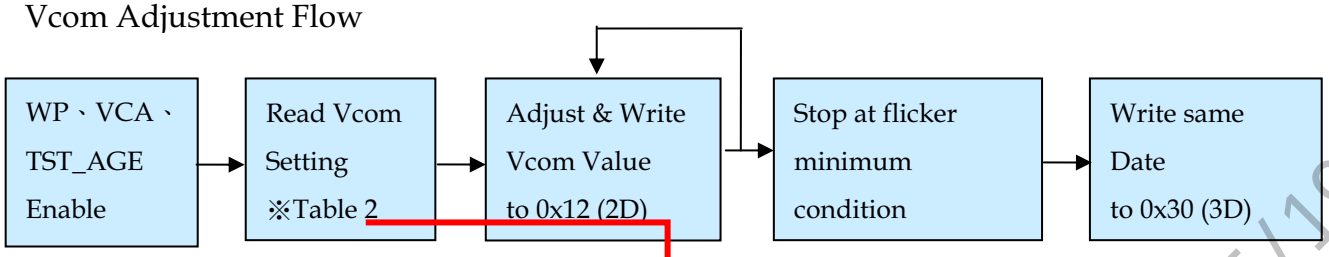
(2) Adjustment method: (Digital V-com)

Programmable memory IC is used for Digital V-com adjustment in this model. INX provide Auto Vcom tools to adjust Digital V-com. The detail connection and setting instruction, please directly contact with Account FAE or refer INX Auto V-com adjustment OI. Below items is suggested to be ready before Digital V-com adjustment in customer LCM line.

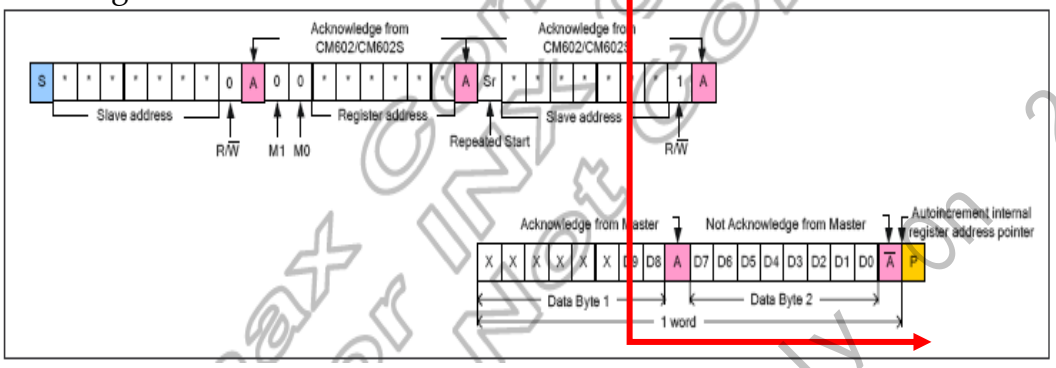
a. USB Sensor Board.

b. Programmable software

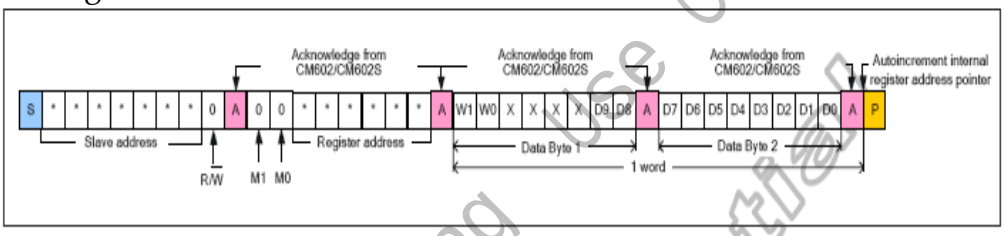
Vcom Adjustment Flow



Reading one indexed word



Writing a word



Vcom Value

Register Address	Register Description
0x12	VCOM1 BK1 (2D)
0x30	VCOM1 BK2 (3D)

Vcom Value adjustable

Register Address	Register Description
0x18	VCOM1 Min BK1 (2D)
0x19	VCOM1 Max BK1 (2D)
0x31	VCOM1 Min BK2 (3D)
0x32	VCOM1 Max BK2 (3D)

5. INTERFACE TIMING

5.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram. (Ta = 25 ± 2 °C)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Frequency	Data Clock	1/Tc	70	74.3	80	MHZ	(1)
V-by-One Receiver	Data skew between each area (A/B)	Tblock	-0.06	—	0.06	H	(2)
	Intra-Pair skew		-0.3	—	0.3	UI	(3)
	Inter-pair skew		-5	—	5	UI	(4)
	Spread spectrum modulation range	F_{clkin_mod}	1/Tc-0.5%	—	1/Tc+0.5%	MHz	(5)
	Spread spectrum modulation frequency	F_{SSM}	—	—	30	KHz	

5.1.1 Timing spec for Frame Rate = 100Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		Fr6	94	100	106	Hz	
	3D mode		Fr6	188	200	212	Hz	(6)
Vertical Active Display Term (4 Lan,960X2160 Active Area)	2D Mode	Total	Tv	2200	2250	2790	Th	Tv=Tvd+Tvb
		Display	Tvd	2160	2160	2160	Th	—
		Blank	Tvb	40	90	630	Th	—
	3D Mode	Total	Tv	1116	1125	1396	Th	(6)
		Display	Tvd	1080	1080	1080	Th	
		Blank	Tvb	36	45	316	Th	
Horizontal Active Display Term (4 Lan,960X2160 Active Area)	2D Mode	Total	Th	270	285	300	Tc	Th=Thd+Thb
		Display	Thd	240	240	240	Tc	—
		Blank	Thb	30	45	60	Tc	—
	3D Mode	Total	Th	270	285	300	Tc	Th=Thd+Thb
		Display	Thd	240	240	240	Tc	—
		Blank	Thb	30	45	60	Tc	—

5.1.2 Timing spec for Frame Rate = 120Hz

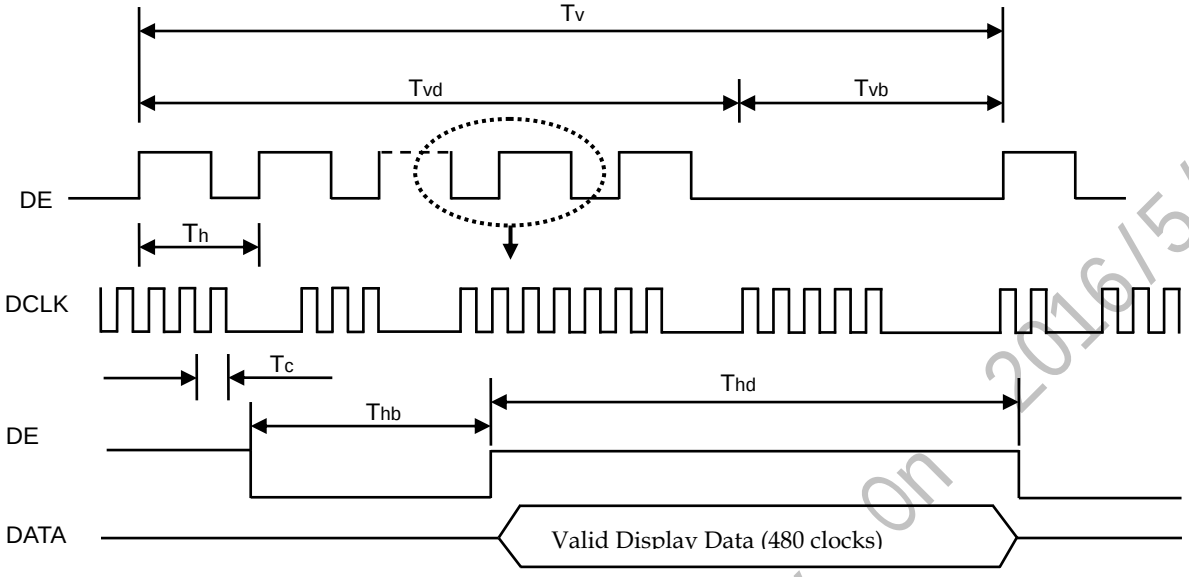
Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		Fr6	114	120	126	Hz	
	3D mode		Fr6	228	240	252	Hz	(6)
Vertical Active Display Term (4 Lan,960X2160 Active Area)	2D Mode	Total	Tv	2200	2250	2790	Th	Tv=Tvd+Tvb
		Display	Tvd	2160	2160	2160	Th	—
		Blank	Tvb	40	90	630	Th	—
	3D Mode	Total	Tv	1116	1125	1200	Th	(6)
		Display	Tvd	1080	1080	1080	Th	
		Blank	Tvb	36	45	120	Th	
Horizontal Active Display Term (4 Lan,960X2160 Active Area)	2D Mode	Total	Th	270	285	300	Tc	Th=Thd+Thb
		Display	Thd	240	240	240	Tc	—
		Blank	Thb	30	45	60	Tc	—
	3D Mode	Total	Th	270	285	300	Tc	Th=Thd+Thb
		Display	Thd	240	240	240	Tc	—
		Blank	Thb	30	45	60	Tc	—

Note (1) Please make sure the range of pixel clock has follow the below equation:

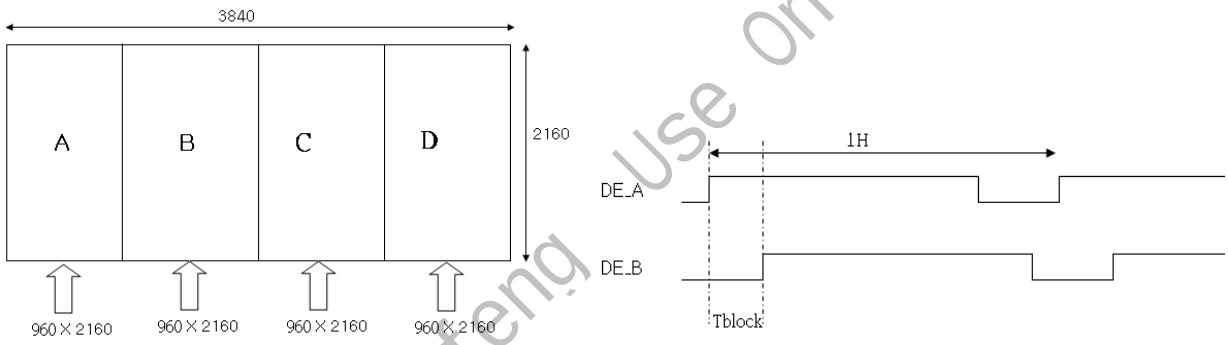
$Fclkin(max) \geqq Fr6 \times Tv \times Th$

$Fr5 \times Tv \times Th \geqq Fclkin(min)$

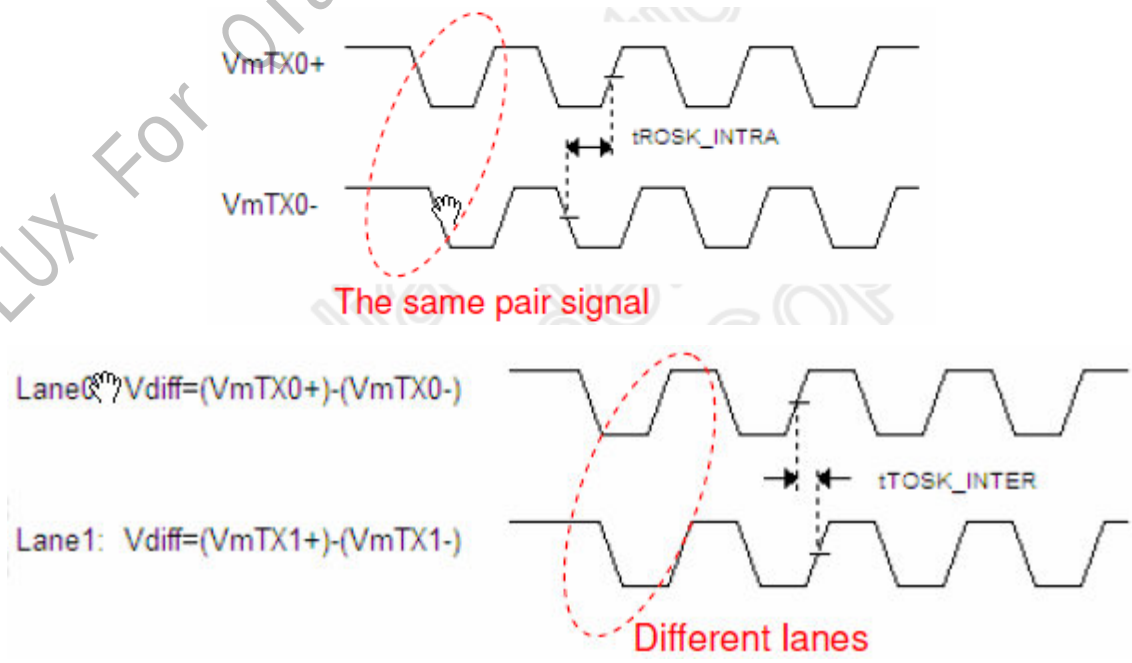
INPUT SIGNAL TIMING DIAGRAM



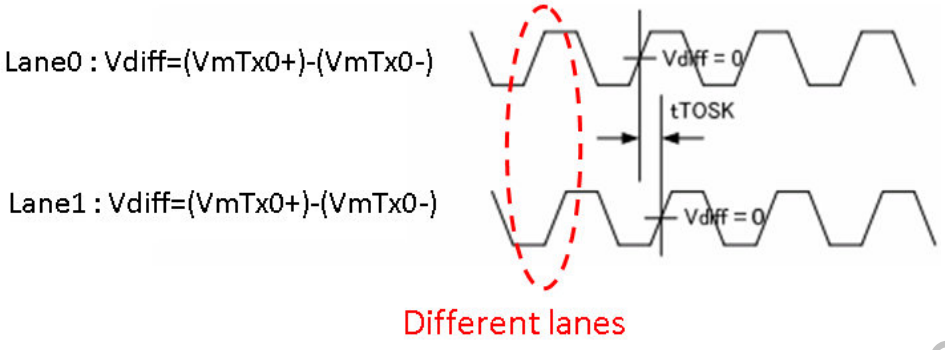
Note (2) Data skew between areas.



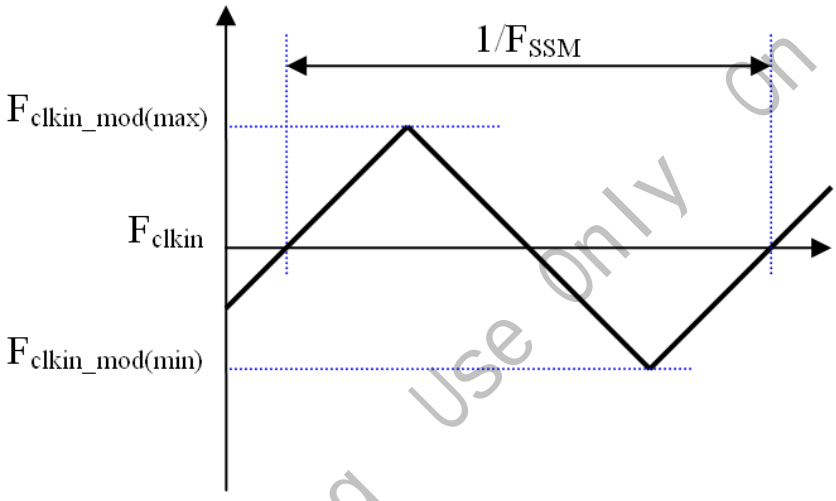
Note (3) V-by-One HS Inter-pair skew.



Note (4) V-by-One HS Inter-pair skew.



Note (5) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (6) In 3D 240Hz mode, the input timing is defined as

3D Input		3D Output
Ln1	-->	Ln1
Ln2	-->	Ln2, Ln3
Ln1080	-->	Ln2158, Ln2159
---		Ln2160 = Black

5.2 V by One Input Signal Timing Diagram

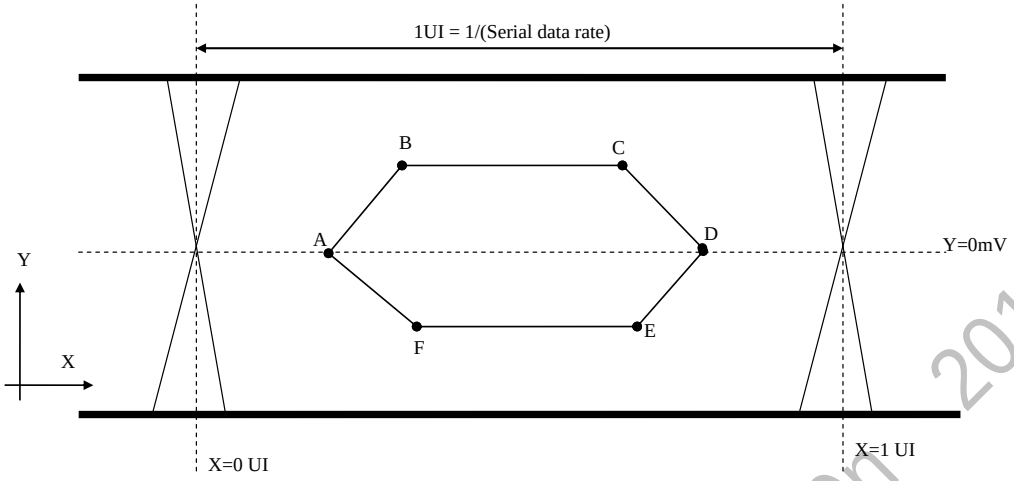


Table 1 Eye Mask Specification

	X [UI]	Y [mV]	Note
A	0.25	0	(1)
B	0.3	50	(1)
C	0.7	50	(1)
D	0.75	0	(1)
E	0.7	-50	(1)
F	0.3	-50	(1)

Note (1) Input levels of V-by-One HS signals are comes from "V-by-One HS Stander Ver.1.4"

5.3 BYTE LENGTH AND COLOR MAPPING OF V-BY-ONE HS

Packer input & Unpacker output		30bpp RGB (10bit)
Byte 0	D[0]	R[2]
	D[1]	R[3]
	D[2]	R[4]
	D[3]	R[5]
	D[4]	R[6]
	D[5]	R[7]
	D[6]	R[8]
	D[7]	R[9]
Byte 1	D[8]	G[2]
	D[9]	G[3]
	D[10]	G[4]
	D[11]	G[5]
	D[12]	G[6]
	D[13]	G[7]
	D[14]	G[8]
	D[15]	G[9]
Byte 2	D[16]	B[2]
	D[17]	B[3]
	D[18]	B[4]
	D[19]	B[5]
	D[20]	B[6]
	D[21]	B[7]
	D[22]	B[8]
	D[23]	B[9]
Byte 3	D[24]	X
	D[25]	X
	D[26]	B[0]
	D[27]	B[1]
	D[28]	G[0]
	D[29]	G[1]
	D[30]	R[0]
	D[31]	R[1]

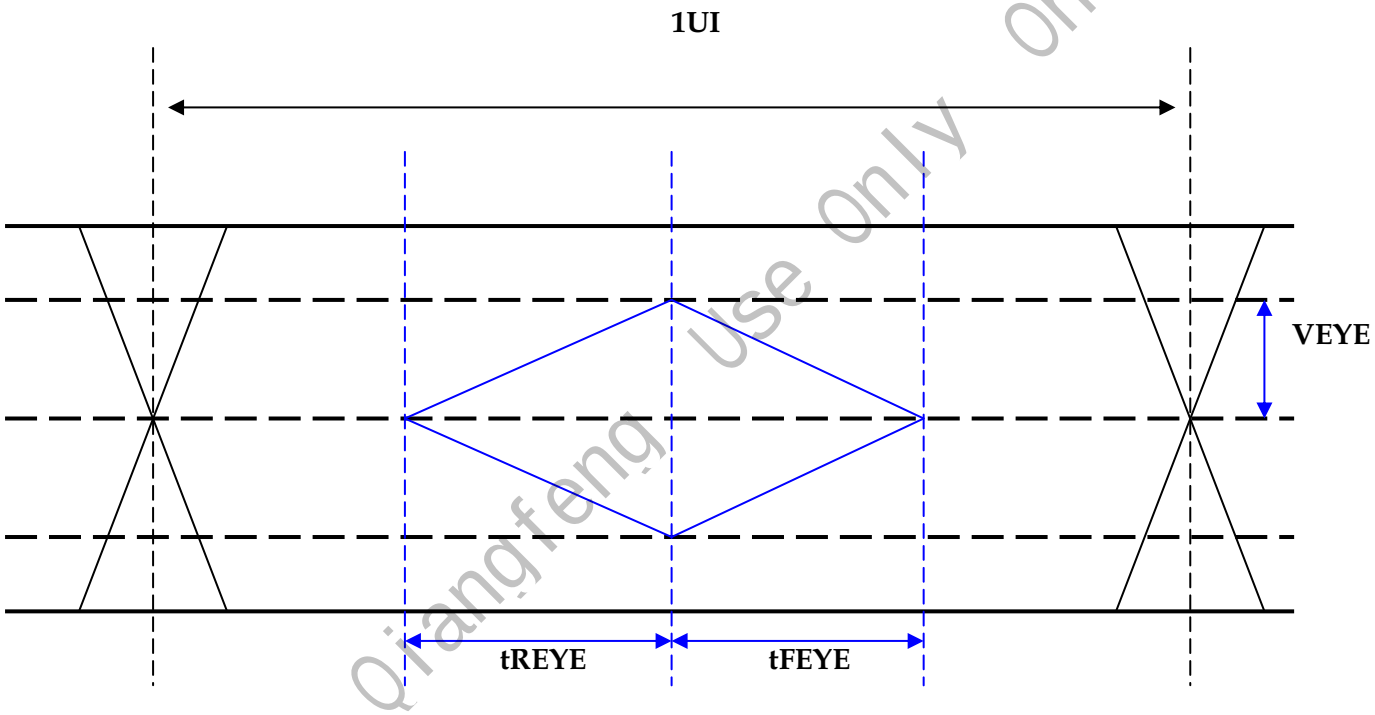
5.4 CMPI eye Timing Diagram

(1) CMPI AC Electrical Characteristics

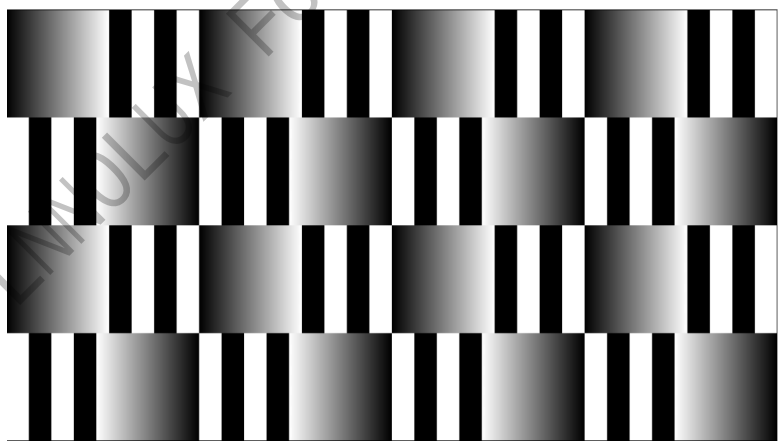
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Effective Veye Rising Time	tREYE	0.2	-	-	UI	
Effective Veye Falling Time	tFEYE	0.2	-	-	UI	
Effective Veye Level	VEYE	75	-	-	mV	

Note (1) CMPI EYE diagram must be in above spec. If your application is not in our spec. . INX can not guarantee Display and function normal.

Note (2) Eye timing diagram

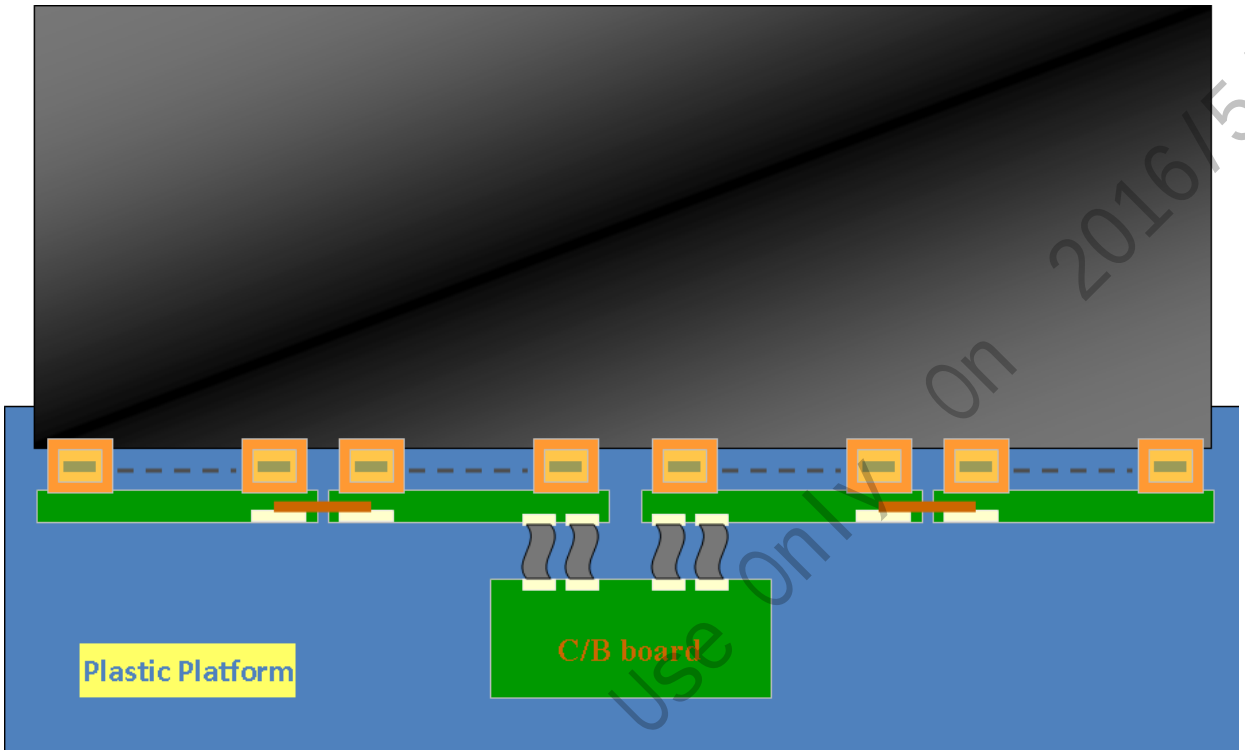


Note (3) Eye diagram measure pattern



Note (4)measure instrument : Lecroy Wave Runner 640Zi (4G/40GS) , Lecroy WL-PBUS D420 (4G) C/B & X/B connect FFC: Impedance Control is 100 +/- 10% (ohm)

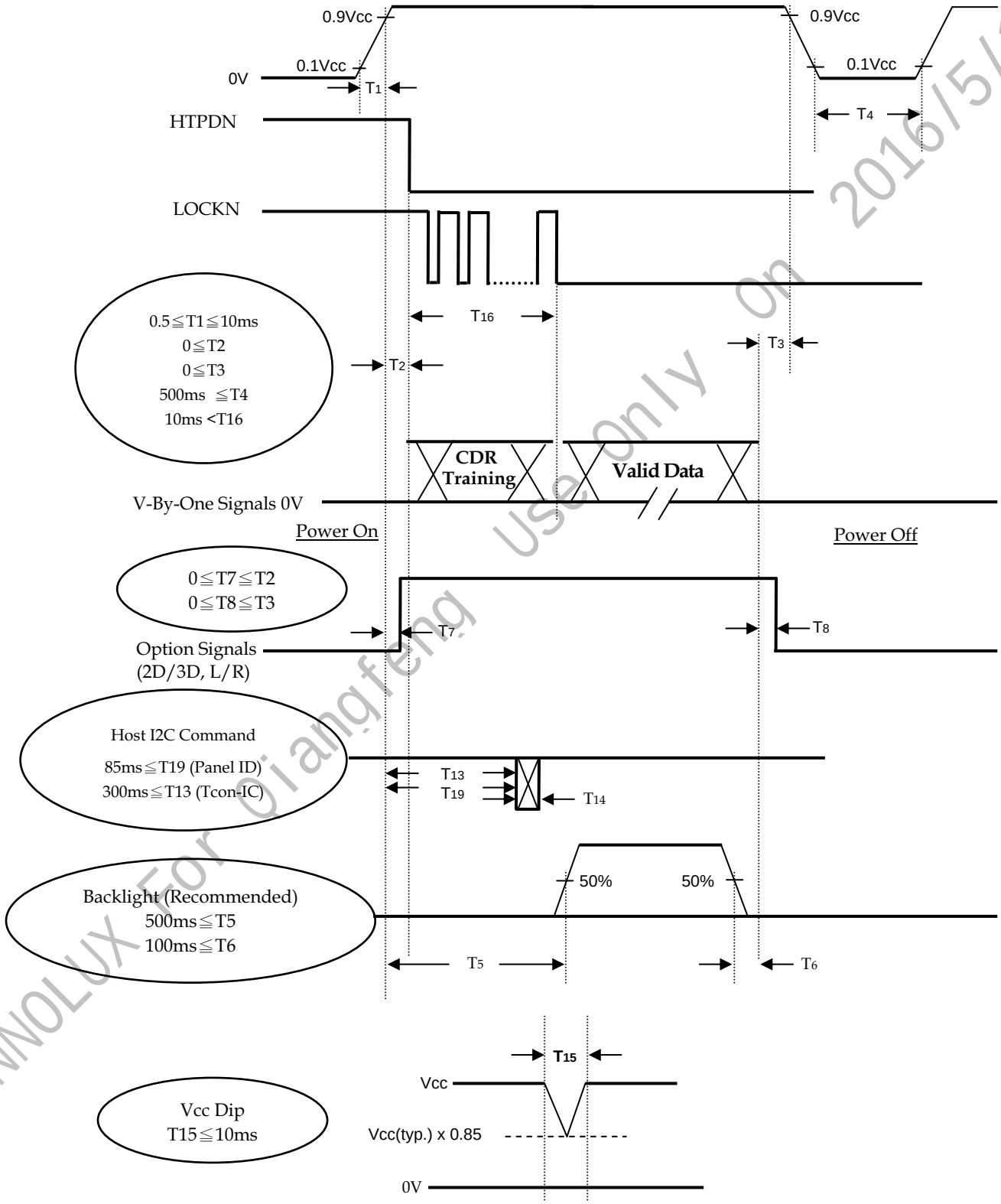
Note (5)CMPI eyes diagram measure pattern



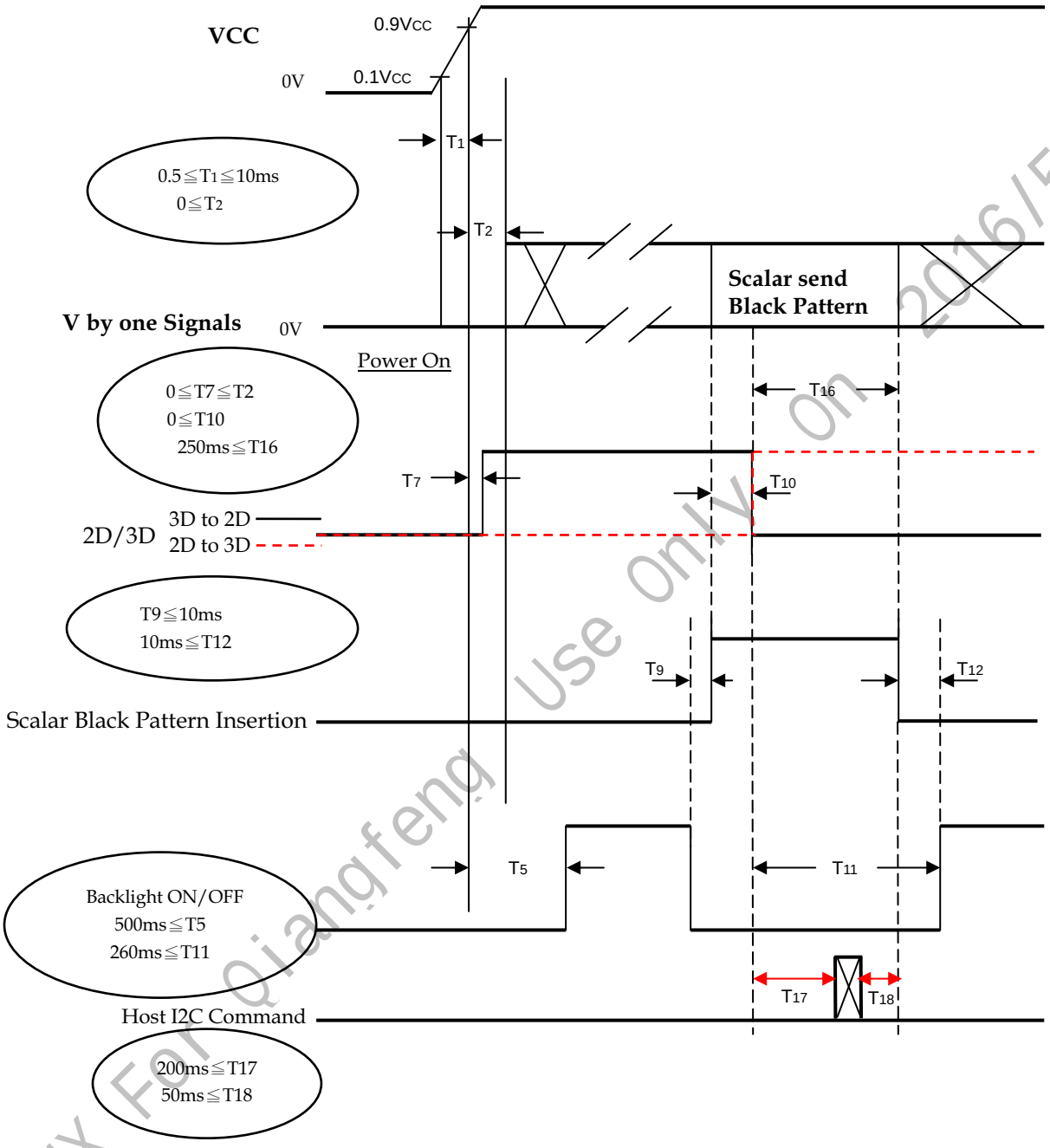
5.5 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 °C)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



5.6 2D/3D MODE CHANGE SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0,that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

Note (6) When 2D/3D mode is changed, TCON will insert black pattern internally. During black insertion, TCON would load required optical table and TCON parameter setting. The black insertion time should be longer than 250ms because TCON must recognize 2D or 3D format and set the correct parameter..

Note (7) Vcc must decay smoothly when power-off.

Note (8) T5 Backlight turn on time depend on T14 command length+T13

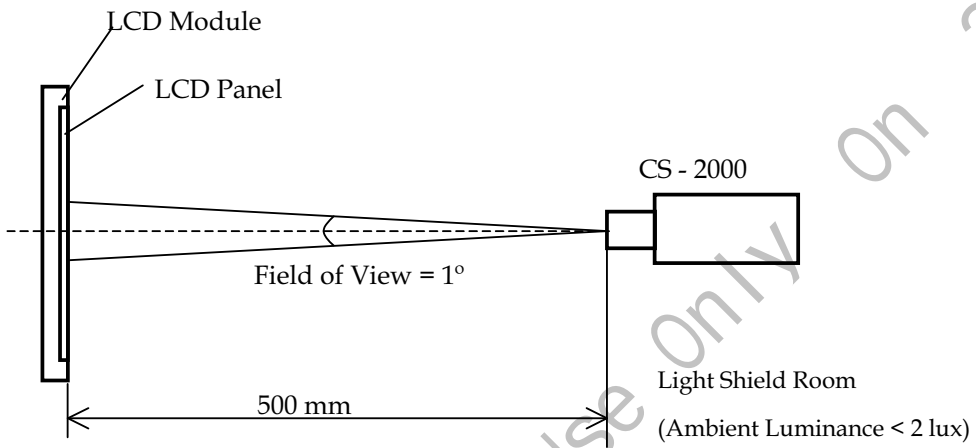
Note (9) The time between I2C commands must be greater than 10 frames at least.

6. OPTICAL CHARACTERISTICS

6.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12V±1.2	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



6.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx	θ_x=0°, θ_Y =0° Viewing Angle at Normal Direction Standard light source "C"	Typ. -0.03	(0.672)	Typ. +0.03	-	(0)
		Rcy			(0.319)		-	
	Green	Gcx			(0.264)		-	
		Gcy			(0.615)		-	
	Blue	Bcx			(0.136)		-	
		Bcy			(0.094)		-	
	White	Wcx			(0.295)		-	
		Wcy			(0.345)		-	
Transmittance		T%	θ_x=0°, θ_Y =0° with INX module	(4.4)	(4.9)		%	(5)
Transmittance Variation		δT				1.3		(6)
Contrast Ratio		CR		(2800)	(4000)	-	-	(1),(3)
Response Time		Gray to gray	θ_x=0°, θ_Y =0° with INX Module	-	6.5	13	ms	(1),(4)
Viewing Angle	Horizontal	θ_x+	CR>10 With INX module	-	89	-	Deg.	(1),(2)
		θ_x-		-	89	-		
	Vertical	θ_Y+		-	89	-		
		θ_Y-		-	89	-		
Transmission direction of the up polarizer		Φ_{up-P}	-	-	90	-	Deg.	(7)

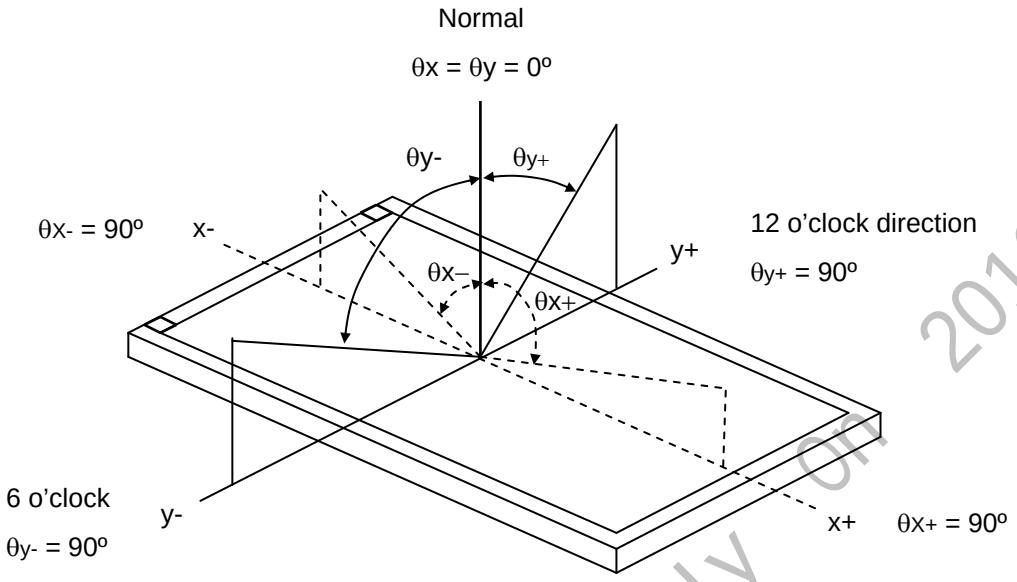
Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltage are based on suitable gamma voltages. The calculating method is as following:

1. Measure Module's and BLU's spectrum at center point. White and R,G,B are with signal input. BLU(for 100'' new R LED testing BLU) is supplied by INX.
2. Calculate cell's spectrum.
3. Calculate cell's chromaticity by using the spectrum of standard light source "C".

Note (1) Light source is the BLU which supplied by INX (for 100'' new R LED testing BLU) and the cell driving voltage are based on suitable gamma voltages..

Note (2) Definition of Viewing Angle (θx, θy) :

Viewing angles are measured by Autronic Conoscope Cono-80 (or Eldim EZ-Contrast 160R)



Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

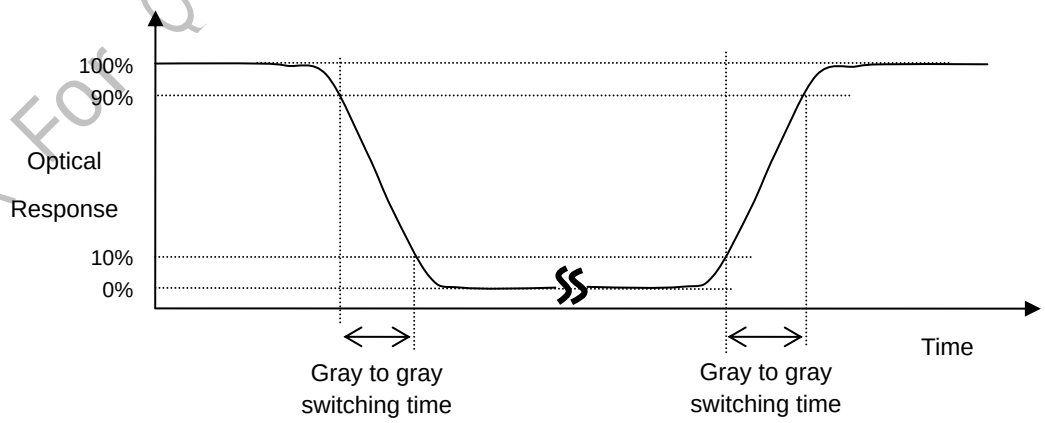
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L1023}}{\text{Surface Luminance of L0}}$$

L1023 : Luminance of gray level 1023

L0 : Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (5).

Note (4) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Note (5) Definition of Transmittance (T%) :

Measure the transmittance at 5 points.

Light source is the BLU which contains three diffuser sheets and the cell driving voltage are based on suitable gamma voltages.

Transmittance (T%) = Average $[T(1), T(2), T(3), T(4), T(5)]$

The transmittance of each point can be calculated by the following expression.

$$T(X) = \frac{L255\,(X)\ \text{of LCD module}}{\text{Luminance}\,(X)\ \text{of BLU}} \times 100\%$$

L255: Luminance of gray level 255

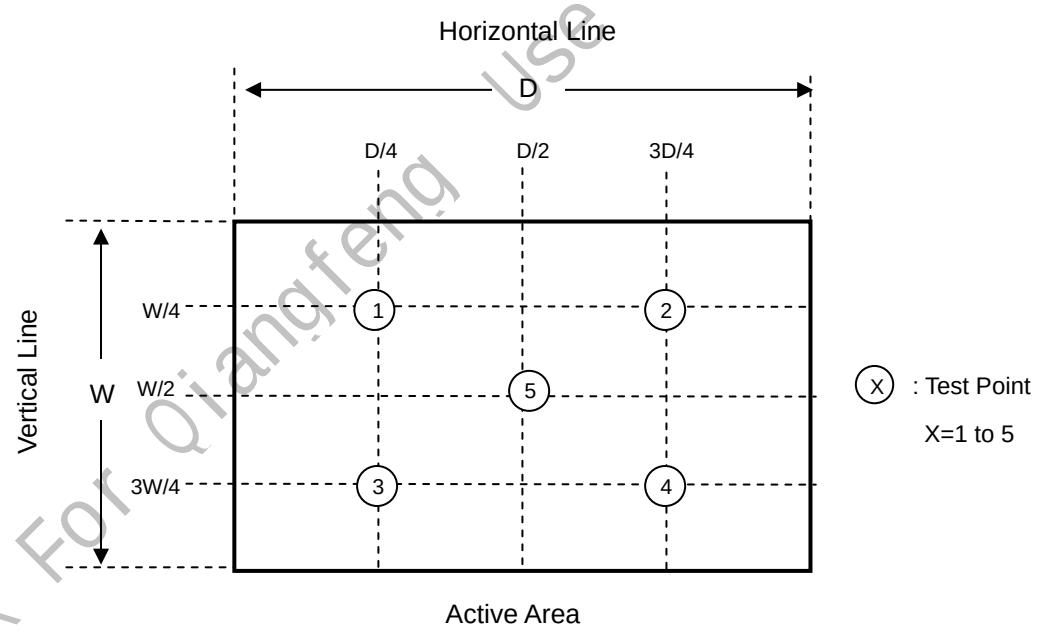
T(X) is corresponding to the point X1~X5 at the figure in Note (6).

Note (6) Definition of Transmittance Variation (δT) :

Measure the transmittance at 5 points.

$$\text{Transmittance Variation } (\delta T) = \frac{\text{Maximum}\,[\,T(1), T(2), T(3), T(4), T(5)\,]}{\text{Minimum}\,[\,T(1), T(2), T(3), T(4), T(5)\,]}$$

T(X) is calculated as Note(5).



7. PRECAUTIONS

7.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply improper or unbalanced force such as bending or twisting to open cells during assembly.

[2] It is recommended to assemble or to install an open cell into a customer's product in clean working areas. The dust and oil may cause electrical short to an open cell or worsen polarizers on an open cell.

[3] Do not apply pressure or impulse to an open cell to prevent the damage.

[4] Always follow the correct power-on sequence when an open cell is assembled and turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5] Do not design sharp-pointed structure / parting line / tooling gate on the plastic part of a COF (Chip on film), because the burr will scrape the COF.

[6] If COF would be bended in assemble process, do not place IC on the bending corner.

[7] The gap between COF IC and any structure of BLU must be bigger than 2 mm. This can prevent the damage of COF IC.

[8] The bezel opening must have no burr and be smooth to prevent the surface of an open cell scraped.

[9] The bezel of a module or a TV set can not contact with force on the surface of an open cell. It might cause light leakage or scrape.

[10] In the case of no FFC or FPC attached with open cells, customers can refer the FFC / FPC drawing and buy them by self.

[11] It is important to keep enough clearance between customers' front bezel/backlight and an open cell. Without enough clearance, the unexpected force during module assembly procedure may damage an open cell.

[12] Do not plug in or unplug an I/F (interface) connector while an assembled open cell is in operation.

[13] Use a soft dry cloth without chemicals for cleaning, because the surface of the polarizer is very soft and easily scratched.

[14] Moisture can easily penetrate into an open cell and may cause the damage during operation.

[15] When storing open cells as spares for a long time, the following precaution is necessary.

[15.1] Do not leave open cells in high temperature and high humidity for a long time. It is highly recommended to store open cells in the temperature range from 0 to 35℃ at normal humidity without condensation.

[15.2] Open cells shall be stored in dark place. Do not store open cells in direct sunlight or fluorescent light environment.

[16] When ambient temperature is lower than 10ºC, the display quality might be reduced.

[17] Unpacking (Cartons/Tray plates) in order to prevent open cells broken:

[17.1] Moving tray plates by one operator may cause tray plates bent which may induce open cells broken. Two operators carry one carton with their two hands. Do not throw cartons/tray plates, avoid any impact on cartons/tray plates, and put down & pile cartons/tray plates gently.

[17.2] A tray plate handled with unbalanced force may cause an open cell damaged. Trays should be completely put on a flat platform.

[17.3] To prevent open cells broken, tray plates should be moved one by one from a plastic bag.

[17.4] Please follow the packing design instruction, such as the maximum number of tray stacking to prevent the deformation of tray plates which may cause open cells broken.

[17.5] To prevent an open cell broken or a COF damaged on a tray, please follow the instructions below:

[17.5.1] Do not peel a polarizer protection film of an open cell off on a tray

[17.5.2] Do not install FFC or LVDS cables of an open cell on a tray

[17.5.3] Do not press the surface of an open cell on a tray.

[17.5.4] Do not pull X-board when an open cell placed on a tray.

[18] Unpacking (Hard Box) in order to prevent open cells broken:

[18.1] Moving hard boxes by one operator may cause hard boxes fell down and open cells broken by abnormal methods. Two operators carry one hard box with their two hands. Do handle hard boxes carefully, such as avoiding impact, putting down, and piling up gently.

[18.2] To prevent hard boxes sliding from carts and falling down, hard boxes should be placed on a surface with resistance.

[18.3] To prevent an open cell broken or a COF damaged in a hard box, please follow the instructions below:

[18.3.1] Do not peel a polarizer protection film of an open cell off in a hard box.

[18.3.2] Do not install FFC or LVDS cables of an open cell in a hard box.

[18.3.3] Do not press the surface of an open cell in a hard box.

[18.3.4] Do not pull X-board when an open cell placed in a hard box.

[19] Handling – In order to prevent open cells, COFs , and components damaged:

[19.1] The forced displacement between open cells and X-board may cause a COF damaged. Use a fixture tool for handling an open cell to avoid X-board vibrating and interfering with other components on a PCBA & a COF.

[19.2] To prevent open cells and COFs damaged by taking out from hard boxes, using vacuum jigs to take out open cells horizontally is recommended.

[19.3] Improper installation procedure may cause COFs of an open cell over bent which causes damages. As installing an open cell on a backlight or a test jig, place the bottom side of the open cell first on the backlight or the test jig and make sure no interference before fitting the open cell into the backlight/the test jig.

[19.4] Handle open cells one by one.

[20] Avoid any metal or conductive material to contact PCB components, because it could cause electrical damage or defect.

[21] The suggestion of removing polarizer-protection film is illustrated as following

[21.1] Scan COF on the left side (Figure 1)

Remove slowly and follow the direction : from left-up to right-down

[21.2] Scan COF on the right side (Figure 2)

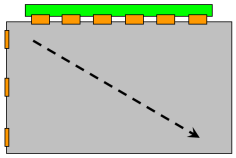
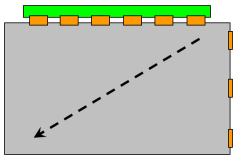
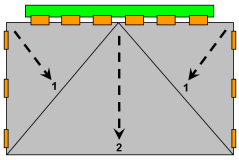
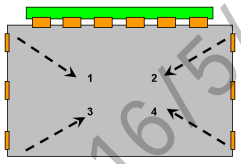
Remove slowly and follow the direction : from right-up to left-down

[21.3] Scan COF on the left and right side (Figure 3)

Remove slowly and follow the direction as marked by 1 and 2.

[21.4] Scan COF on the left and right side (Figure 4)

Remove slowly and follow the direction as marked by 1, 2, 3 and 4.

Figure 1	Figure 2	Figure 3	Figure 4
			

7.2 SAFETY PRECAUTIONS

[1] If the liquid crystal material leaks from the open cell, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[2] After the end of life, open cells are not harmful in case of normal operation and storage.

9. PACKAGING

9.1 PACKAGING SPECIFICATIONS

(1) 4 LCD TV Panels / 1 Box

(2) Box dimensions : 2435 (L) X 1585 (W) X 103 (H)mm

(3) Weight : approximately 75 Kg (4 panels per box)

(4) 24 LCD TV Panels / 1 Group

(5) Only full stack will be packed in the carton inner box.

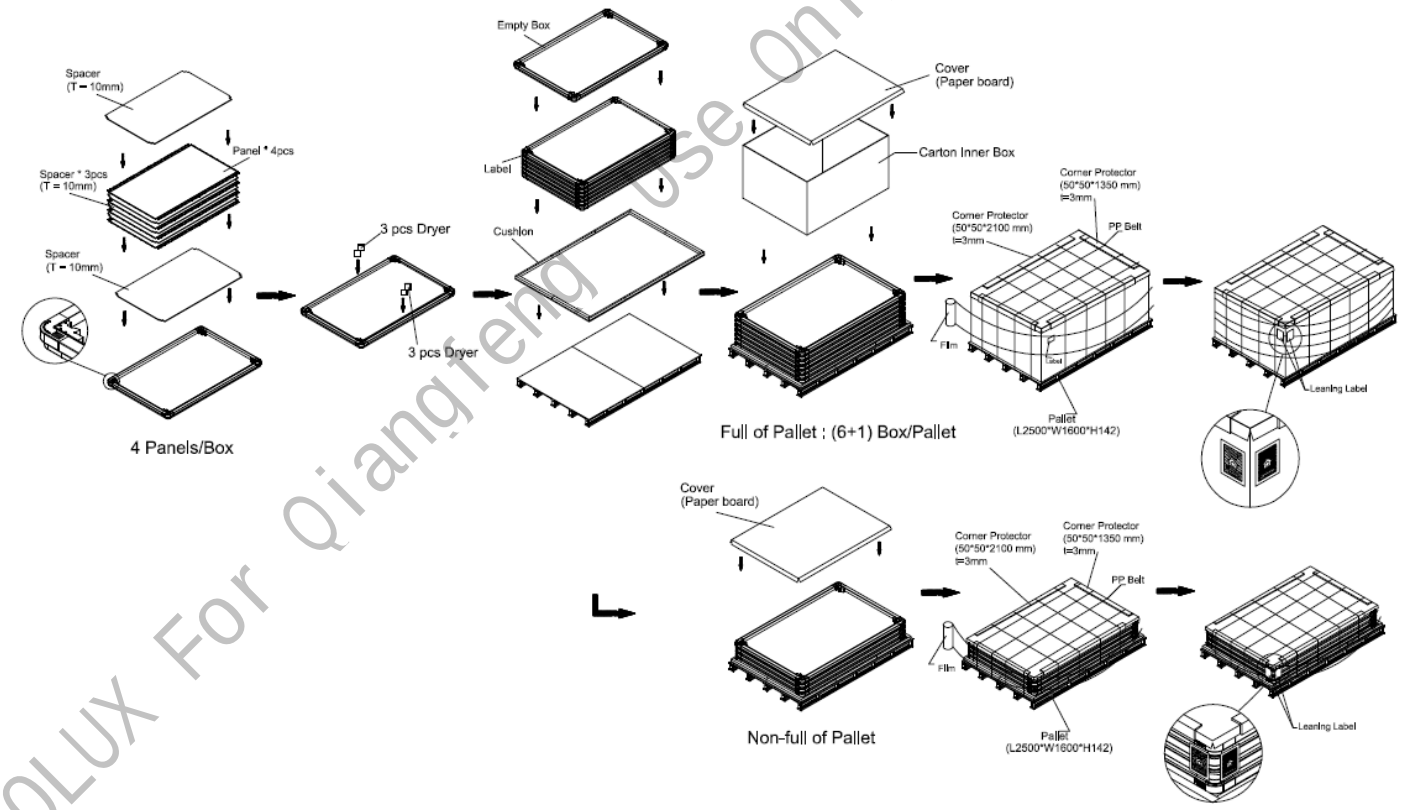
(6) Please fill up the container to avoid any cargo be damaged.

(7) INX recommends to follow the same packing method as described in 9.2.

(8) By air or express delivery, it's necessary to pack wooden box in the outer layer of the goods under one stack.

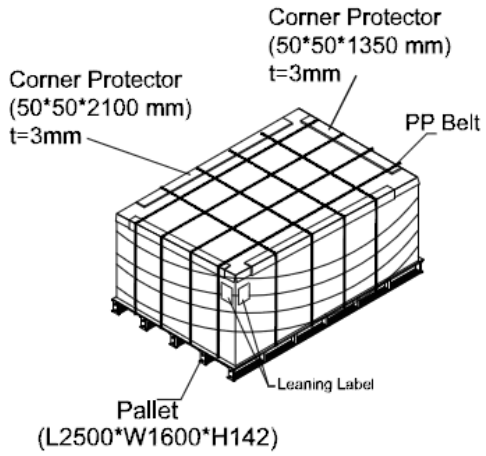
9.2 PACKAGING METHOD

Packaging method is shown in following figures.



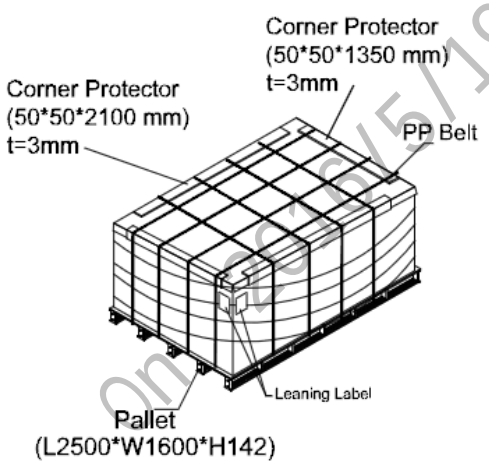
Shipping Mode

Sea / Land Transportation



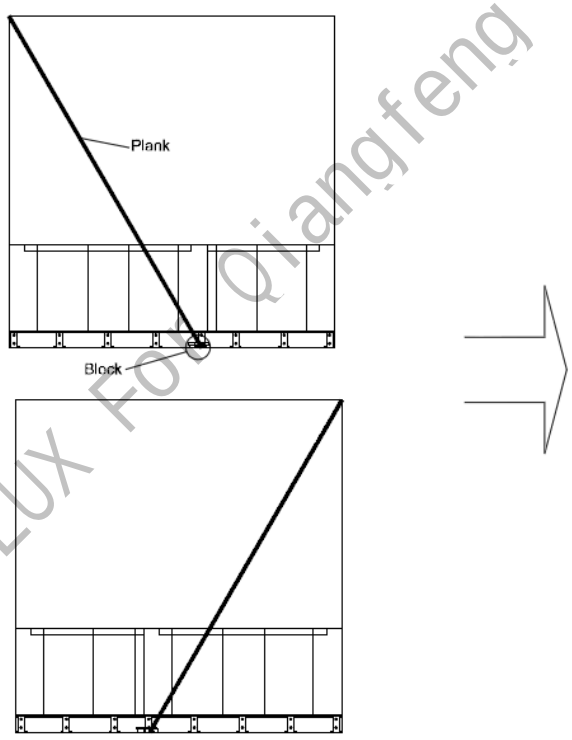
(6+1) Box/Pallet

Air Transportation

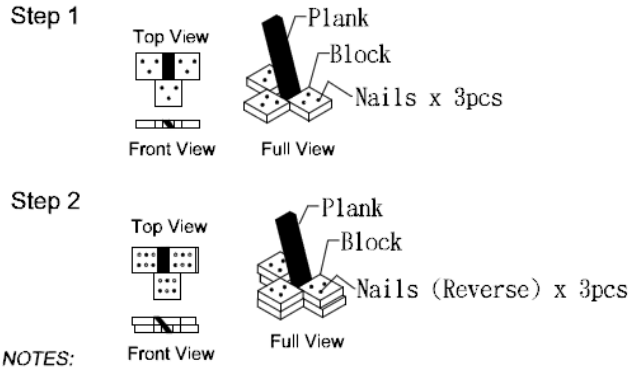


(6+1) Box/Pallet

The Fixed Way of Block and Plank in the Container Tail



(Front View)



NOTES:

1. Block:
- *(1) Wood : L=150mm , W=70mm , H=45mm (With Wood Pallet)*
- *(2) Paper : L=100mm , W=100mm , H=30mm (With Plywood Pallet)*

2. Plank:
- *(1) Wood (With Wood Pallet)*
  - *HQ Container : L=2840mm , W=88mm , H=45mm*
  - *GP Container : L=2575mm , W=88mm , H=45mm*
  - *Common : L=3130mm , W=88mm , H=45mm*
- *(2) Plywood (With Plywood Pallet)*
  - *HQ Container : L=2860mm , W=90mm , H=45mm*
  - *GP Container : L=2480mm , W=90mm , H=45mm*
  - *Common : L=3130mm , W=90mm , H=45mm*

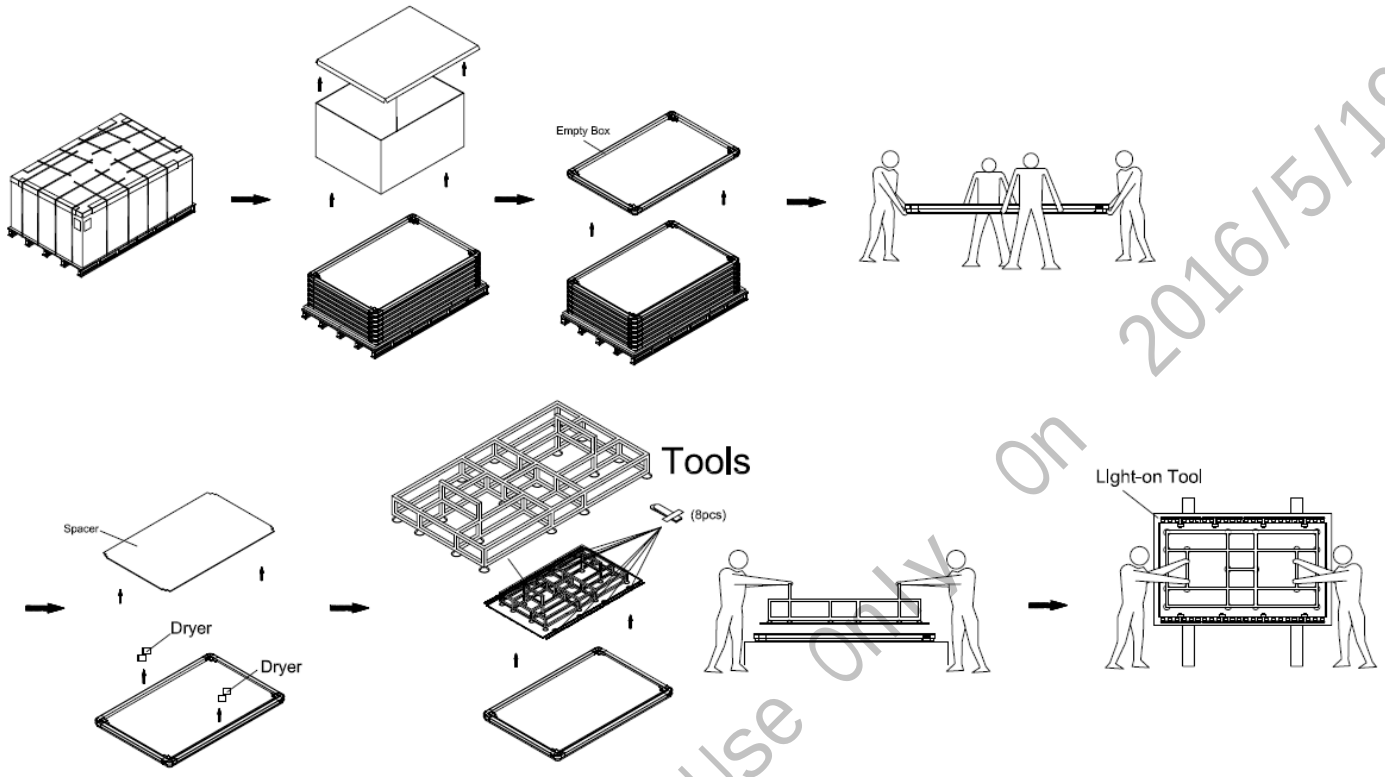
3. Nail : Coil Nail (FC-70) , Length 67mm

4. The Dimension Tolerance of Block, Plank and Nail is ±5%

5. The plank need to close the sidewall of the container and container flooring to fixed

9.3 UN-PACKAGING METHOD

Un-packaging method is shown as following figures.



10. DEFINITION OF LABELS

10.1 OPEN CELL LABEL

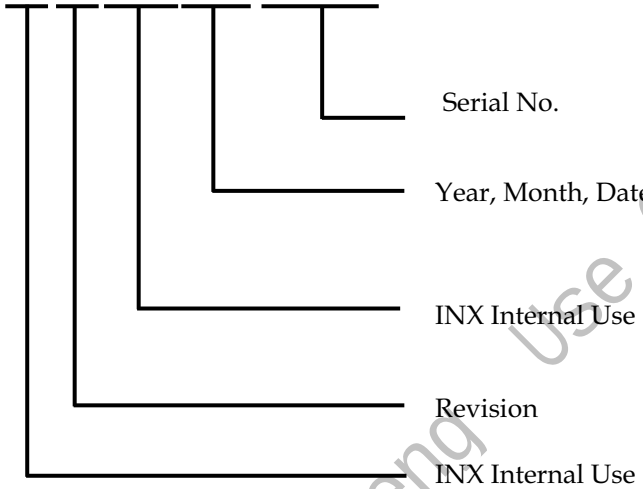
The barcode nameplate is pasted on each open cell as illustration for INX internal control.

Figure.9-1 Serial No. Label on SPWB

Model Name : VA00DK1-QS1

Revision : Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID : X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date :

Year: 2010=0, 2011=1,2012=2…etc.

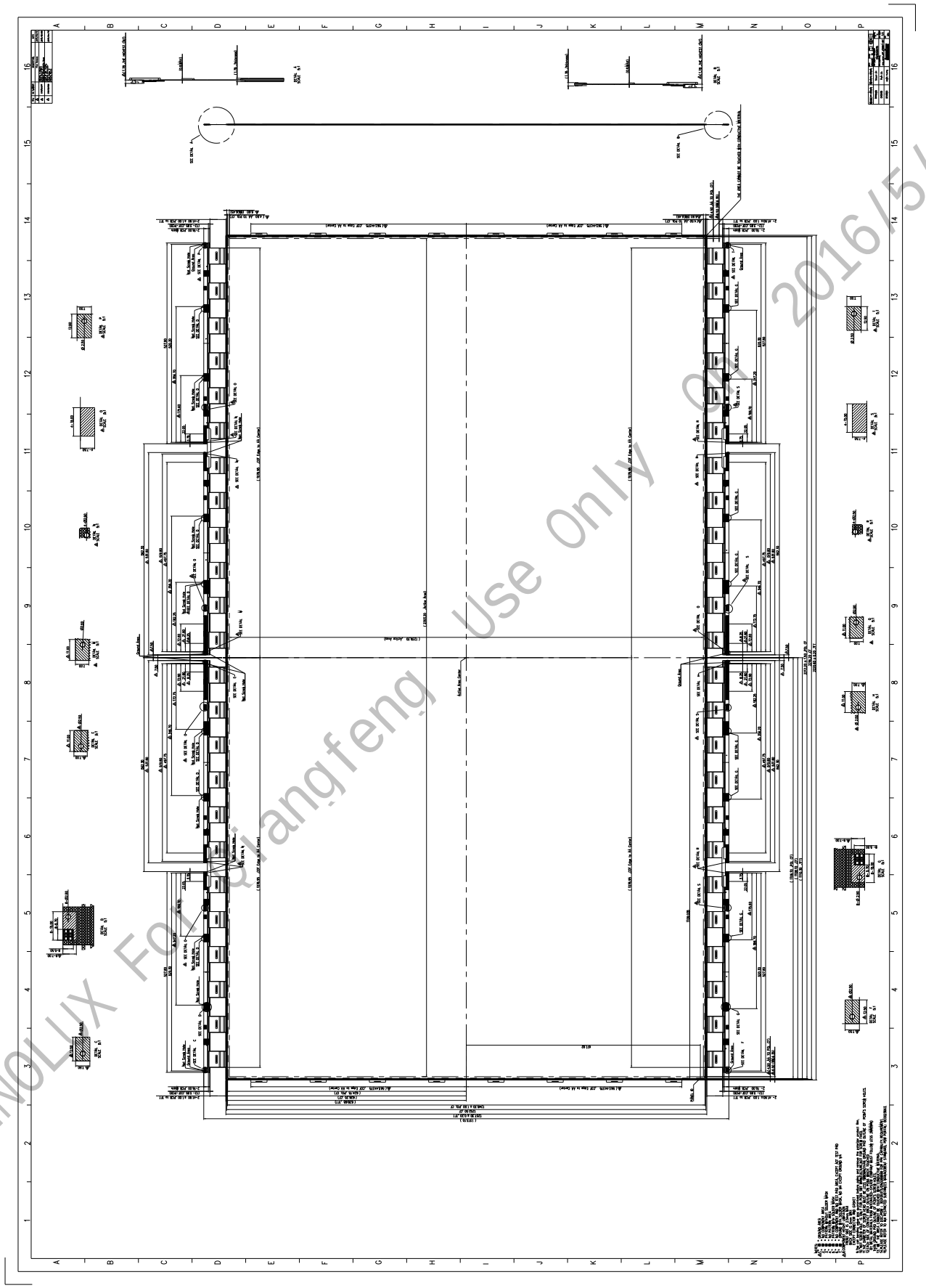
Month: 1~9, A~C, for Jan. ~ Dec.

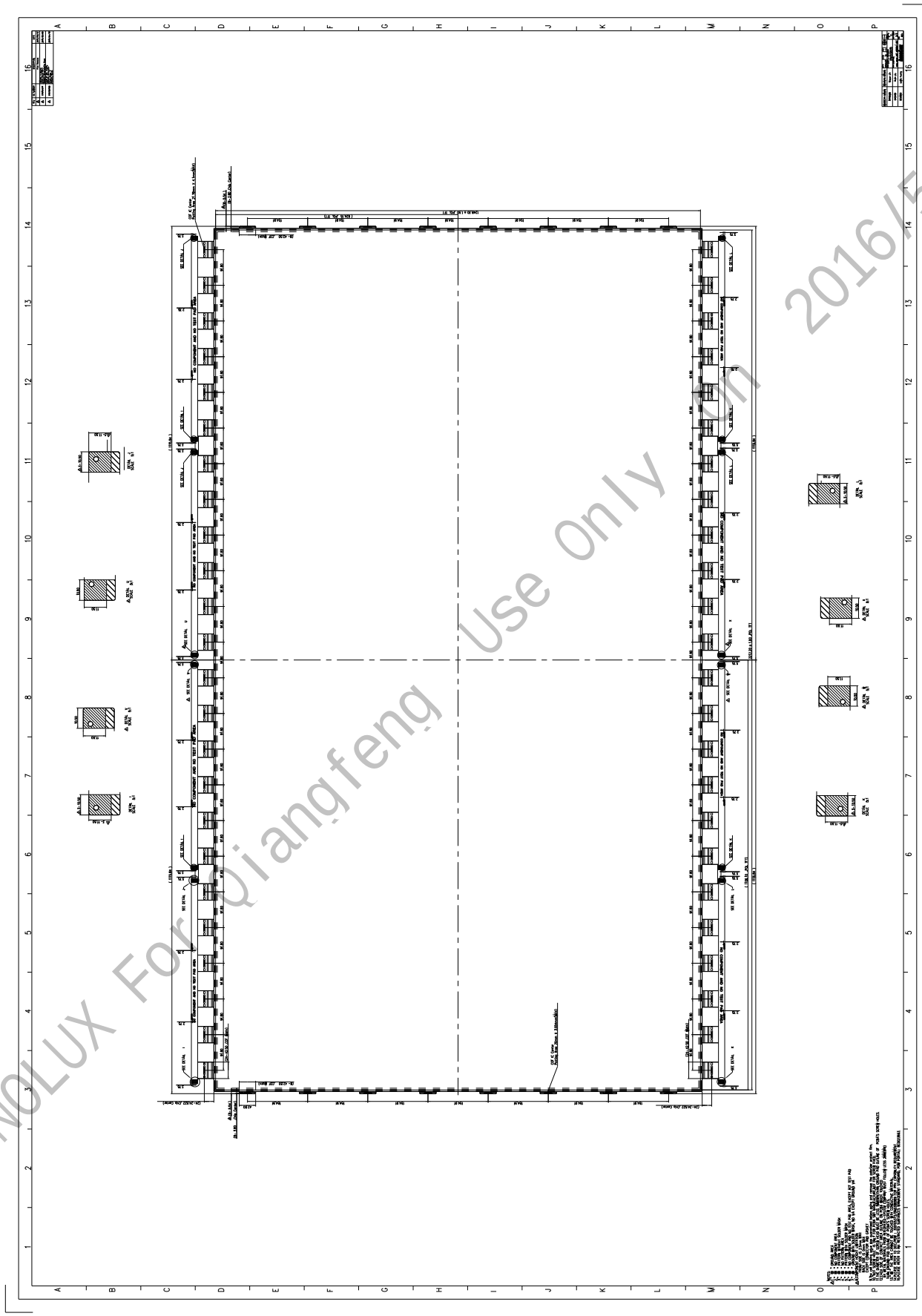
Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

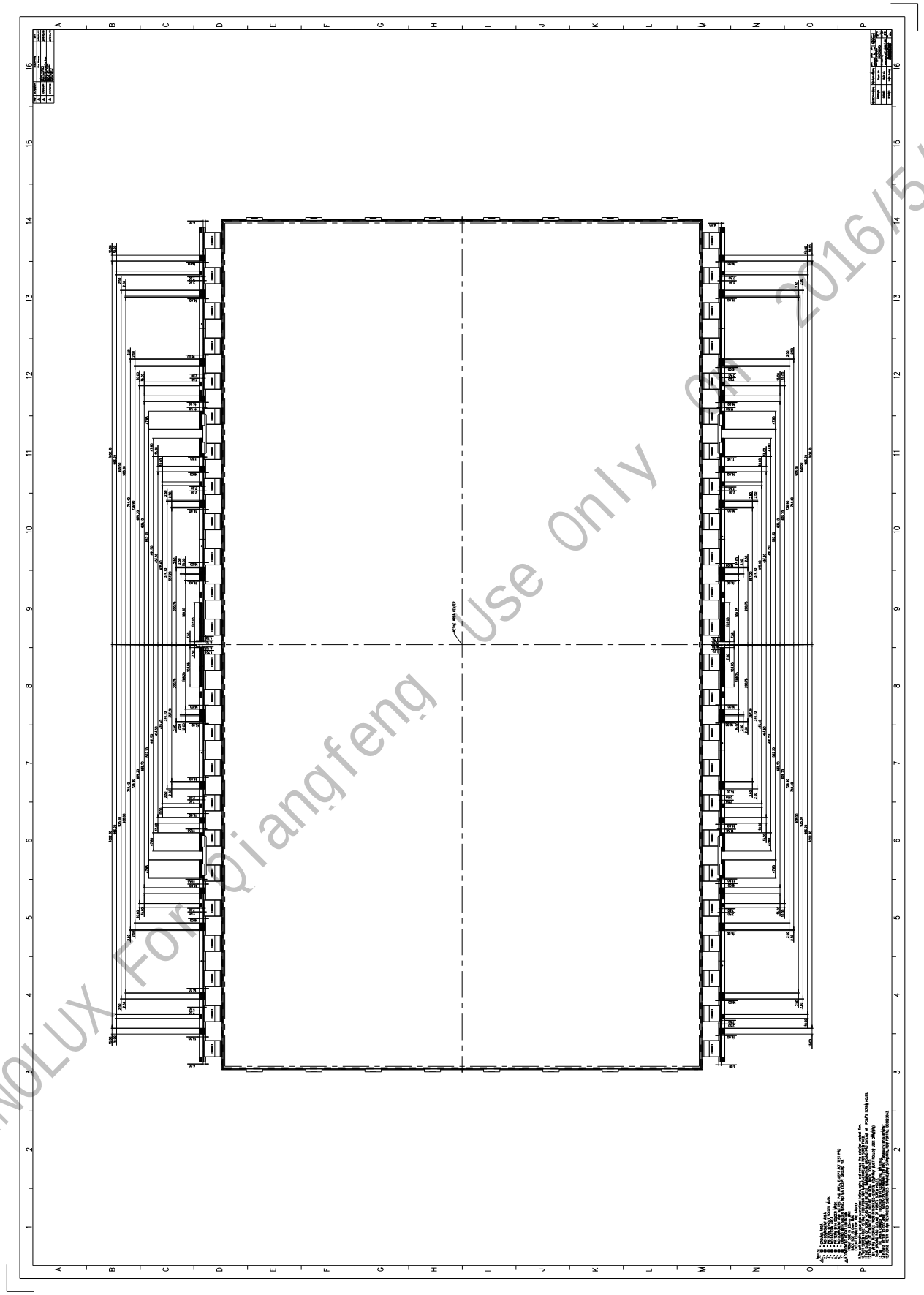
Revision Code : Cover all the change

Serial No.: Manufacturing sequence of product

11. MECHANICAL CHARACTERISTIC







Appendix A

A.1 I2C timing

Symbol	Parameter	Min.	Max.	Unit
t_{SU-STA}	Start setup time	250	-	ns
t_{HD-STA}	Start hold time	250	-	ns
t_{SU-DAT}	Data setup time	80	-	ns
t_{HD-DAT}	Data hold time	0	-	ns
t_{SU-STO}	Stop setup time	250	-	ns
t_{BUF}	Time between Stop condition and next Start condition	500	-	ns