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CORPORATE RESEARCH AND DEVELOPMENT GROUP

SPECIFICATION

MODEL No.

DEVICE SPECIFICATION FOR

TFT-LCD Open Cell

JE695R3HD9K

CUSTOMER'S APPROVAL

DATE _____

BY _____

Title & Department _____

Company _____

PRESENTED

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RECORDS OF REVISION

MODEL No. : JE695R3HD9K

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SPEC No.	DATE	REVISED No.	PAGE	SUMMARY	NOTE
LD-S21105	Jan. 25. 2021	-	-		1st ISSUE
LD-S21105A	Jan. 25. 2021	A	13	Add suffix code	2nd ISSUE
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1. Application

This specification applies to the color TFT-LCD Open-Cell “JE695R3HD9K”.

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2. Overview

This Open Cell (JE695R3HD9K) is a color active matrix LCD Open Cell incorporating amorphous silicon TFT (Thin Film Transistor), Polarizers, Source-PWBs, Source-Drivers, and Gate-Drivers are made arrayed in glass BM area. Graphics and texts can be displayed on a 3840 x RGB x 2160 dots panel with one billion colors by input USI-T signal from an adequate C-PWB.

[Caution]

*This Open Cell is designed only for the Single Frame Rate driving.

*You should design thermal conductive interface pad enough to radiate heat from IC in Source-Drivers.

This Open-Cell has below features.

- 4K2K (3840 x BGR x 2160) High Resolution
- VNB (Very Narrow Bezel) amorphous-silicon-TFT-LCD-Panel
- UV2A High Contrast and Transmittance Pixel Aperture
- Gate on array (GOA) structure
- Bezel-less processing for full flat TV design
- Wide-View angle with MPD (Multi-Pixel-Driving)
- USI-T High Speed Driver Interface Technology

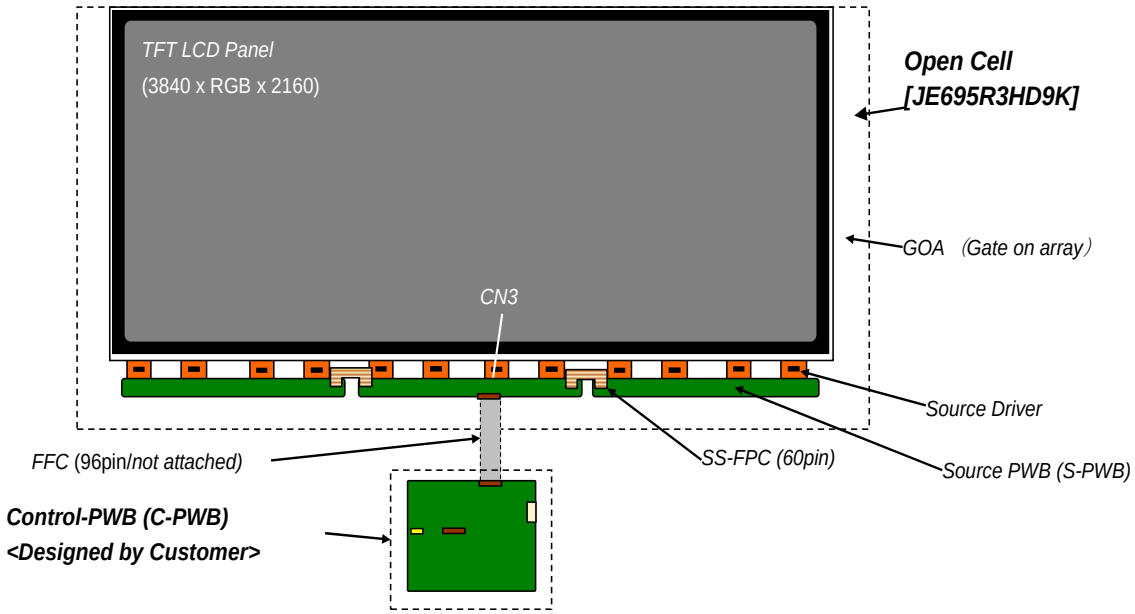


Fig.1 Diagram of Open Cell

3. Mechanical Specifications

Parameter	Specification	Unit
Display size (Active Area)	1535.232 (H) x 871.560 (V)	mm
	176.538 (Diagonal) [69.5'']	cm
Pixel Format	3840 (H) x 2160 (V) (1pixel = R + G + B dot)	pixel
Pixel pitch	0.3998(H) x 0.4035 (V)	mm
Pixel configuration	B,G,R vertical stripe	-
Display mode	Normally black	-
Outline dimensions [1)]	1545.232 (H) x 927.7 (V) x 3.0 (D) *Cell Thickness: 1.47	mm
Mass	4.5±0.5	kg
Surface treatment [2)]	- Front polarizer: Low-Haze(less than 5%) Anti-Glare, Hard-Coating(2H and more) - Rear polarizer: Hard-Coating less	-

1) The thickest point is the 60pin-CN on the S-PWB, the display area thickness is shown the outline drawing in Page 18.
2) With the protection film removed.

4. Open Cell Driving Specifications

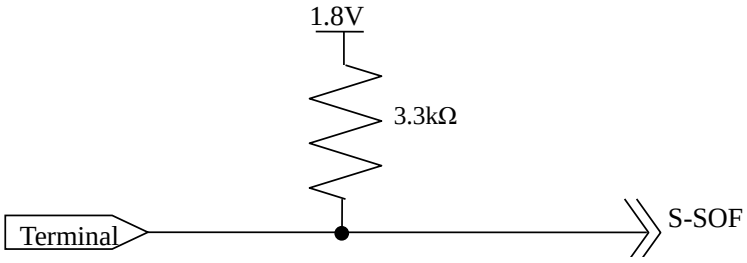
4.1. TFT-LCD panel driving

Interface Signals (CN3)
Connector: 104267-9617 (Molex) or equivalent device

Pin No.	CN3 of S-PWB			
	Symbol	Function	I/O	Remark
1	AVDD	Source analog power supply (VLS/VDD2)	I	
2	AVDD	Source analog power supply (VLS/VDD2)	I	
3	AVDD	Source analog power supply (VLS/VDD2)	I	
4	AVDD	Source analog power supply (VLS/VDD2)	I	
5	AVDD	Source analog power supply (VLS/VDD2)	I	
6	AVDD	Source analog power supply (VLS/VDD2)	I	
7	AVDD	Source analog power supply (VLS/VDD2)	I	
8	AVDD	Source analog power supply (VLS/VDD2)	I	
9	U_H	External Gamma Reference Voltage (VH255)	I	
10	U_L	External Gamma Reference Voltage (VH0)	I	
11	HAVDD	Source Supply Voltage (VDD2M)	I	
12	HAVDD	Source Supply Voltage (VDD2M)	I	
13	L_H	External Gamma Reference Voltage (VL0)	I	
14	L_L	External Gamma Reference Voltage (VL255)	I	
15	FB_2	Connection with FB_1	-	
16	GND	GND	I	
17	SFC1	Shared Forward Channel Control	I	[Note1]
18	GND	GND	I	
19	CH5_B-	SCOF12_USIT DATA0N	I	
20	CH5_B+	SCOF12_USIT DATA0P	I	
21	GND	GND	I	
22	CH5_A-	SCOF11_USIT_DATA0N	I	
23	CH5_A+	SCOF11_USIT_DATA0P	I	
24	GND	GND	I	
25	CH4_B-	SCOF10_USIT_DATA0N	I	
26	CH4_B+	SCOF10_USIT_DATA0P	I	
27	GND	GND	I	
28	CH4_A-	SCOF9_USIT_DATA0N	I	
29	CH4_A+	SCOF9_USIT_DATA0P	I	
30	GND	GND	I	
31	CH3_B-	SCOF8_USIT_DATA0N	I	
32	CH3_B+	SCOF8_USIT_DATA0P	I	
33	GND	GND	I	
34	CH3_A-	SCOF7_USIT_DATA0N	I	
35	CH3_A+	SCOF7_USIT_DATA0P	I	
36	GND	GND	I	
37	CH2_B-	SCOF6_USIT_DATA0N	I	
38	CH2_B+	SCOF6_USIT_DATA0P	I	
39	GND	GND	I	
40	CH2_A-	SCOF5_USIT_DATA0N	I	
41	CH2_A+	SCOF5_USIT_DATA0P	I	
42	GND	GND	I	

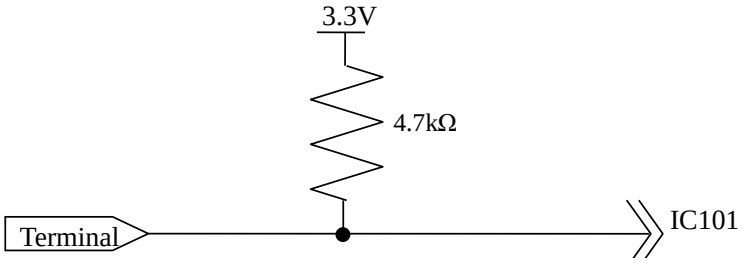
43	CH1_B-	SCOF4_USIT_DATA0N	I	
44	CH1_B+	SCOF4_USIT_DATA0P	I	
45	GND	GND	I	
46	CH1_A-	SCOF3_USIT_DATA0N	I	
47	CH1_A+	SCOF3_USIT_DATA0P	I	
48	GND	GND	I	
49	CH0_B-	SCOF2_USIT_DATA0N	I	
50	CH0_B+	SCOF2_USIT_DATA0P	I	
51	GND	GND	I	
52	CH0_A-	SCOF1_USIT_DATA0N	I	
53	CH0_A+	SCOF1_USIT_DATA0P	I	
54	GND	GND	I	
55	SBC(DSF/SRF)	Shared Bidirectional Channel	I/O	Pull-up [Note1]
56	SEL_EQ_ID	Select EQ mode	I	H: Smart EQ v1.0 L: Hard-wired mode
57	VCCB	Source Logic Supply Voltage (VDD1)	I	+1.8V
58	VCCB	Source Logic Supply Voltage (VDD1)	I	+1.8V
59	VCCA	Source Logic Supply Voltage (VDD1)	I	+1.9V
60	VCCA	Source Logic Supply Voltage (VDD1)	I	+1.9V
61	IO3(HOLD)	SPI Hold/Reset	I	Pull-up [Note2] H: Reset L: Hold
62	SCK	SPI Clock	I	
63	CS	SPI Chip Select	I	Pull-up [Note2]
64	IO0(DI)	SPI data Input	I	
65	IO1(DO)	SPI data Output	O	
66	IO2(WP)	SPI Write Protect	I	H: Protect Disable L: Protect Enable
67	Panel_3.3V(VCC)	Logic power supply	I	+3.3V
68	NC	OPEN	-	
69	VSS(TFT)	OPEN	-	
70	VOFF(GOA)	Gate Low Power Supply	I	
71	VOFF(GOA)	Gate Low Power Supply	I	
72	OPEN	OPEN	-	
73	OPEN	OPEN	-	
74	OPEN	OPEN	-	
75	OPEN	OPEN	-	
76	OPEN	OPEN	-	
77	OPEN	OPEN	-	
78	CK8(CKVB4_GOA)	Gate Clock3	I	
79	CK7(CKVB3_GOA)	Gate Clock2	I	
80	CK6(CKVB2_GOA)	Gate Clock1	I	
81	CK5(CKVB1_GOA)	Gate Clock8	I	
82	CK4(CKV4_GOA)	Gate Clock7	I	
83	CK3(CKV3_GOA)	Gate Clock6	I	
84	CK2(CKV2_GOA)	Gate Clock5	I	
85	CK1(CKV1_GOA)	Gate Clock4	I	
86	STVP1(ST GOA)	Gate Start Pulse (GSP)	I	
87	STVP2(RESET)	Gate End Pulse (GEP)	O	
88	VCOM3	OPEN	-	
89	VCOM2	OPEN	-	
90	VCOM2	OPEN	-	
91	VCOM1(DVR)	TFT-LCD-Panel Common Voltage	I	
92	VCOM1(DVR)	TFT-LCD-Panel Common Voltage	I	
93	NC(FB_VCOM2)	OPEN	-	
94	NC(FB_VCOM1)	OPEN	-	
95	GND	GND	I	
96	FB_1	Connection with FB_2	-	

[Note 1] The equivalent circuit figure of the terminal for SBC:



*SFC & SBC electrical specification is written in page 10.

[Note2] The equivalent circuit figure of the terminal for SPI Hold, CS:



*W25Q32JV(Winbond) is used for De-Mura correction. Please refer to the data sheet about SPI connection detail.

4.2. Interface block diagram

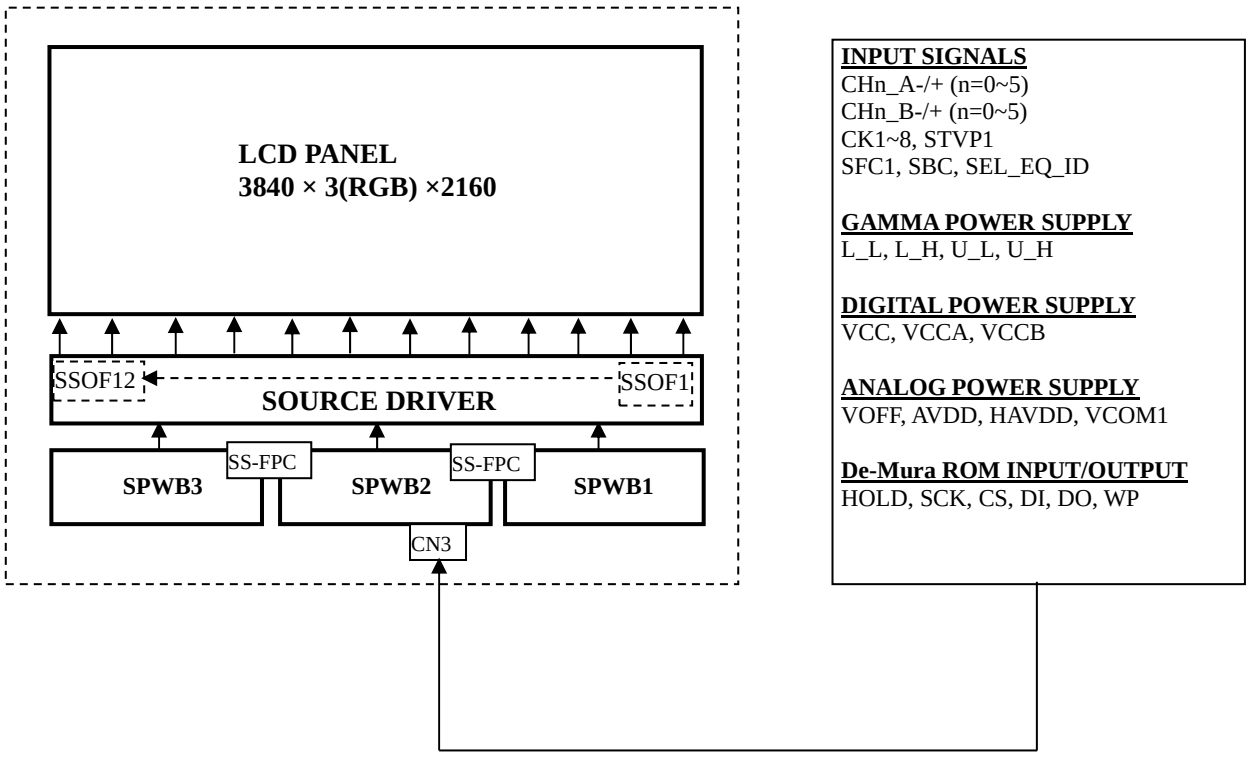
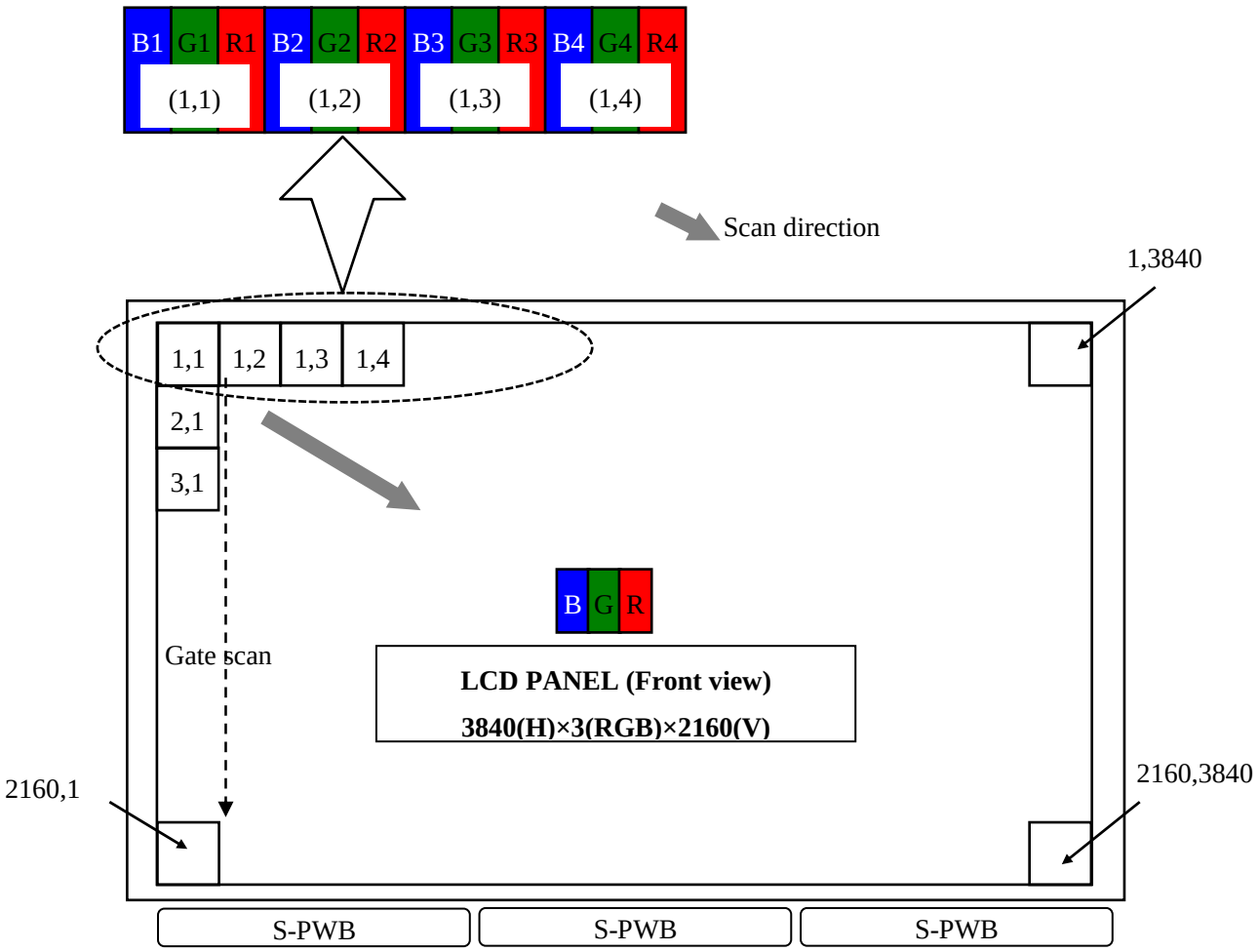


Fig.2 Block Diagram

4.3. Display direction & PWB layout

In this module each subpixel R, G, B is aligned as follows. Three S-PWBs are layout at the bottom side of the screen.



LCD subpixel alignment

Fig.3 Input data signal and display position on the screen

4.4. S-PWB connector to FFC

S-PWB Input Connector (CN3) : 104267-9617 (Molex) or Equivalent one.
Recommended Terminal Figure of FFC is as follows:

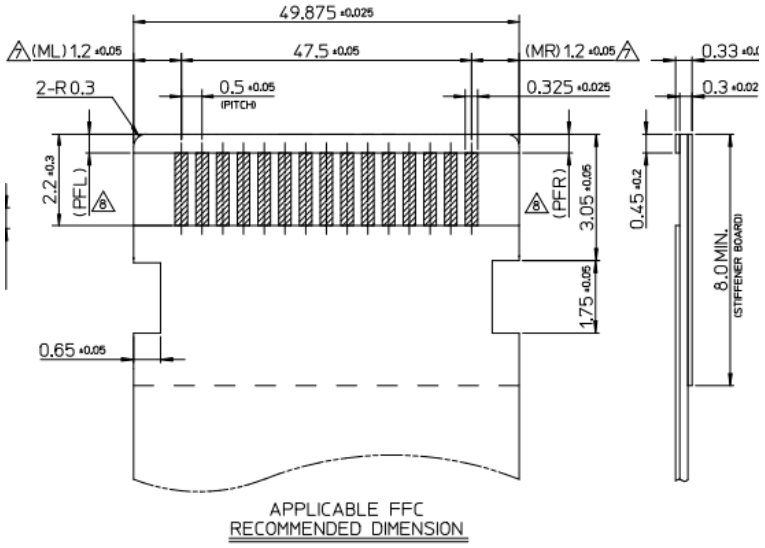


Fig. 4 Recommended Dimension of applicable FFC

5. Adjust TFT-LCD Panel Common voltage (Vcom)

For the prevention of a long-time image sticking of the TFT-LCD panel, the Common Voltage (Vcom) is adjusted to the optimum value for each panel. The VCOM value is stored in Flash on the source-board.

Please do not change the VCOM value as it may adversely affect the panel quality.

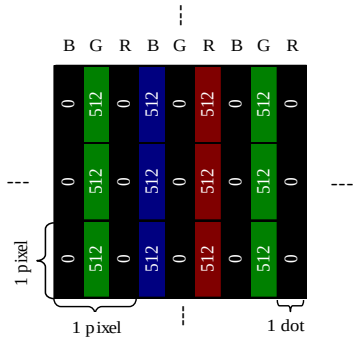


Fig.5 Vcom Tuning Pattern: 1-Source-Line-Stripe

6 Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit	Remark
Driver Supply voltage	VCCA/B	Ta=25ºC	-0.3 ~ 2.2	V	S-Dr.
	AVDD	Ta=25ºC	-0.3 ~ 20.4	V	S-Dr.
	HAVDD	Ta=25ºC	-0.3 ~ 11.3	V	(AVDD-HAVDD=-0.3~11.3)
	U_H, U_L	Ta=25ºC	AVDD-11.3 ~ AVDD+0.3	V	S-Dr.
	L_H, L_L	Ta=25ºC	-0.3 ~ 0.5AVDD	V	S-Dr.
Input voltages	Input Signals	Ta=25ºC	-0.3 ~ (VCCA/B)+0.3	V	CHn_A/B-/+, SFC
Storage temperature (OC)	Tstg	-	-20 ~ +60	ºC	OpenCell Surface
Operation temperature (OC)	Topa	-	0 ~ +50	ºC	

- Humidity 95%RH Max.(at Ta ≦ 40 ºC)
- Maximum wet-bulb temperature 39 ºC or less (at Ta > 40 ºC)
- No condensation.
- Design the module with a maintaining temperature of the panel at 60ºC or less and uniform as much as possible. Otherwise there is possibility to cause several issues such as “Mura” or “Gamma shift”, etc.
- Design the module with a maintaining temperature of Black Mask(BM) area of panel at 70 ºC or less and uniform as much as possible. Otherwise there is possibility to cause functional issue in GOA circuit, which is located at BM area.
- The recommended operating maximum temperature of the Source-Driver-IC is 125 ºC at a chip surface.

7 Electrical Characteristics of Input Signals

7.1 DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Source Dr Logic (USI-T Rx) supply	VCCA	1.62	1.9	1.98	V	
	VCCB	1.62	1.8	1.98	V	
Source Dr Logic dynamic current	ICC1	-	-	14.3	mA	VCCB=1.8V, VCCA=1.9V, $f_{USIDATA}$=1500MHz, CLK1 period=3.7us, each driver
Source Dr Logic (USI-T Rx) dynamic current	ICC1A	Typ-30%	30	Typ+30%		
Source Dr supply voltage	AVDD	15.0	17.3	18.5	V	[Note15]
	HAVDD	0.5AVDD -1.0	8.53	0.5AVDD +1.0	V	AVDD=15.0～18.5V
Source Dr supply Current	AVDD	-	0.2	3.5	A	[Note6]
	HAVDD	-	0.03	0.7	A	[Note6]
	VCCA	-	0.2	0.4	A	[Note6]
	VCCB	-	0.3	0.6	A	[Note6]
Gamma correction voltage	U_H	0.5AVDD and HAVDD+0.2	16.16	AVDD-0.2	V	
	U_L		8.95			
	L_H	GND +0.2	7.93	0.5AVDD and HAVDD-0.2		
	L_L		0.181			
USI-T input offset voltage [Note1]	V_{ICM}	0.3	0.45	0.6	V	VCCA/B==1.62 ~ 1.98V
USI-T differential input data voltage [Note2,3]	V_{ID}	67.5	-	600	mV	
USI-T differential input data peak-to-peak voltage [Note4]	$V_{ID_DIFF_P\text{-}P}$	135	-	1200	mV	
Internal termination resistor	R_T	Typ-15%	110	Typ+15%	Ohm	[Note5]
Input leakage current	I_L	-1	-	1	uA	Without pull-up/down SFC, USIT DATA0P/N
	I_{L2}	-400	-	400		With pull-up/down, , SEL/EQ_ID

[Note1] V_{ICM} is the common mode voltage of the differential input data.
[Note2] The min/max level of V_{ID} includes all the AC fluctuation upon DC level.
[Note3] The min level of V_{ID} means internal min value of USI-T data and the max level of V_{ID} means external max value of the USI-T data in eye diagram, respectively.
[Note4] The conditions of measurement for eye diagram are to remove the driver IC and to attach 100ohm termination resistor on the S-PWB, and to bond a Driver IC on the S-PWB, respectively.
[Note5] R_T is an internal termination resistor (On-Die Termination). Condition is $T_{C,typ}$ (52.5 ºC)
[Note6] TYP current is RMS value when full white is displayed.
Regarding the current consumption of power supply for each display pattern, please see below table.

	Display Pattern				
Power Supply	White	Black	Checker	H-Stripe	V-Stripe
AVDD	1.686 A	0.251 A	1.271 A	1.892 A	1.028 A
HAVDD	0.034 A	0.044 A	0.151 A	0.041 A	0.365 A
VCCA_1.9V	0.169 A	0.166 A	0.176 A	0.171 A	0.166 A
VCCB_1.8V	0.257 A	0.268 A	0.303 A	0.266 A	0.299 A

[Note6] Signal parameter and characteristics

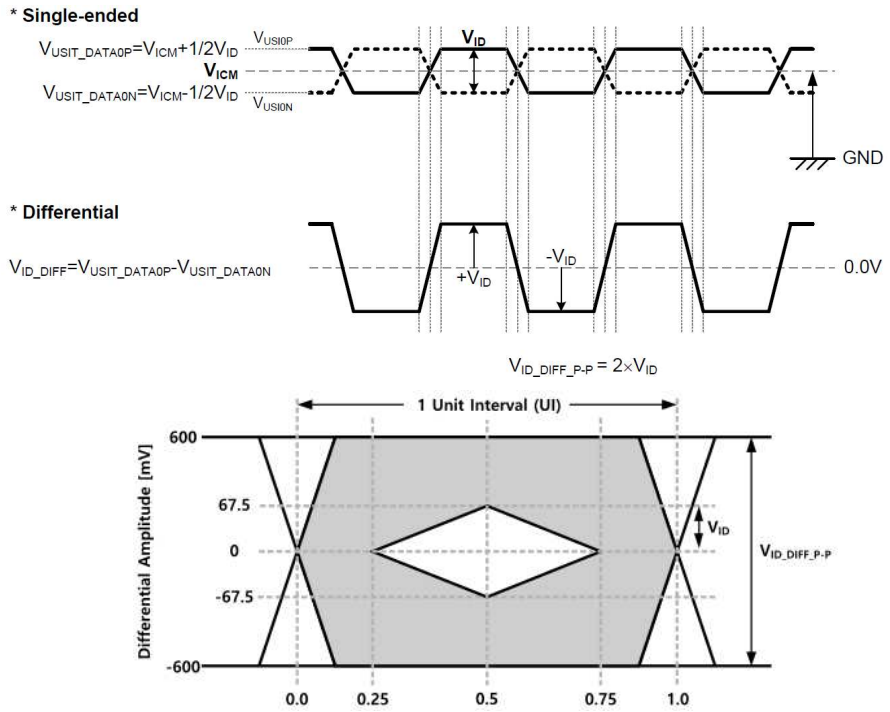


Fig.6 Eye Diagram

< Power sequence >

Source series: GND → VCC=1.8V → Input signals → VLS → HALFVDD

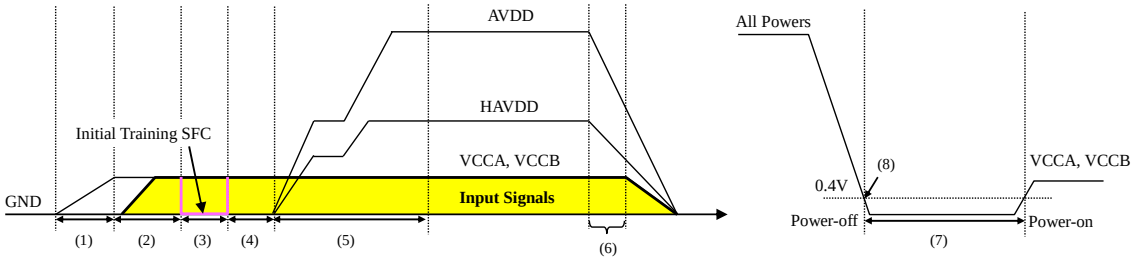
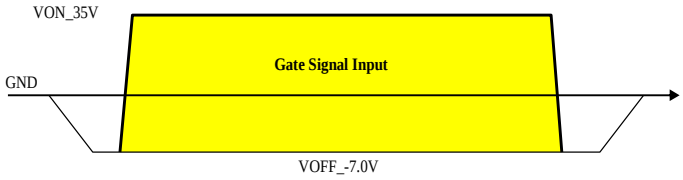


Fig.8 Power sequence

(1) VCCA/B settling time (Max. 5ms). All input signals set to GND level.
(2) VCCA/B should be settled down before the falling edge of SFC input in this period. There is no time limit in this period.
(3) USI-T initialization period (Min. 4500T ~ Max. 40ms). Input signals must be stable.
(4) Delay time from the end of USI-T initialization period to the start of AVDD (Min. 8ms).
Rx logic is initialized in this period.
(5) AVDD & HAVDD settling time (Max. 0.5s).
(6) Power-off sequence begins at these points. Power-off points of VCCA/B are defined as minimum voltage of the recommended operation conditions. The voltage difference of AVDD and HAVDD must be in the absolute maximum ratings defined.
(7) Power-on/off interval: Min.0.8s
(8) At this point, all powers must be less than or equal to 0.4V.

Gate series: GND → VSS= -7.0V → GOA Signal Input



7.2 AC characteristics (Source Input)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
USI-T data frequency	$f_{USIDATA}$	600	-	1500	MHz	
		1.2	-	3	Gbps	
USI-T clock period	t_{USICLK}	3.33	-	8.33	ns	10 x t_{UI} [Note1,2]
USI-T data pulse with	t_{UI}	0.333		0.833		$f_{USIDATA}$=0.6GHz ~ 1.5GHz [Note1,3]
Reference clock phase locking time	t_{LOCK}	4500	-	-	t_{USICLK}	[Note4]
Minimum line blank period	t_{LB}	42	-	-		[Note5]
CLK1 start line prior to the next line data	t_{CLK1}	1				[Note5]
Power-on slope	t_0	-	-	5	ms	[Note4, 7]
Stand-by time between power on and 1st data transfer	t_1	1	-	-		
Training pattern offset time before and after SFC=L	t_2	5	-	-	t_{USICLK}	

[Note1] 1T = 10UI = 1 t_{USICLK}

[Note2] Refer to the below figure.

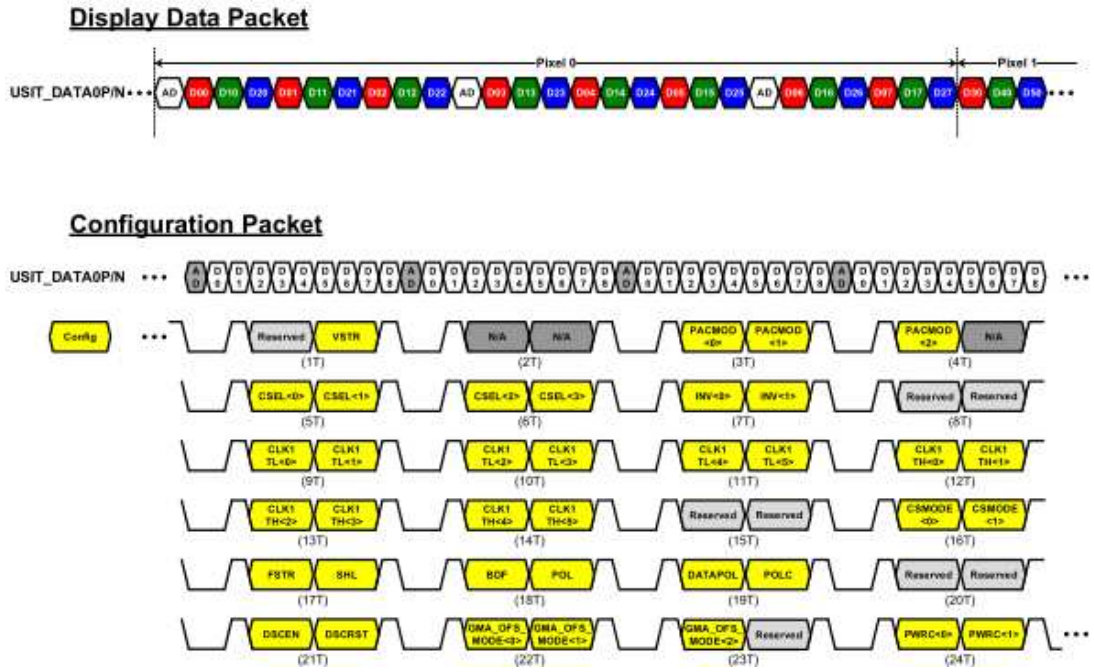


Fig.7 Display anda Configuration Data Packet

[Note3] AC timing parameters, t_{UI}.

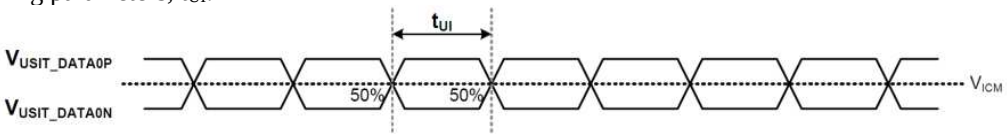


Fig.8 Timing waveform(t_{UL})

[Note4] AC timing parameters, t_0, t_1, t_2, t_{LB} and t_{LOCK}

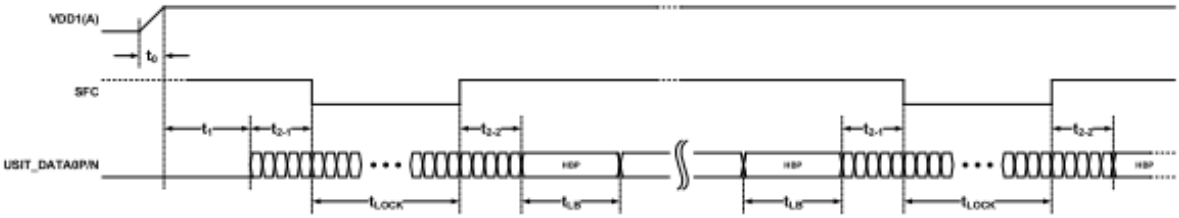


Fig.9 Timing waveform (t_0, t_1, t_2, t_{UL} t_{LB} and t_{LOCK})

$t_{2\text{-}1}$ and $t_{2\text{-}2}$ timing parameters are included in the t_{START} and t_{END}, and in this period, USxO/E_P/N(USIT_DATA0P/N) is the clock training pattern.

[Note5] AC timing parameters, t_{LB}, t_{CLK1}

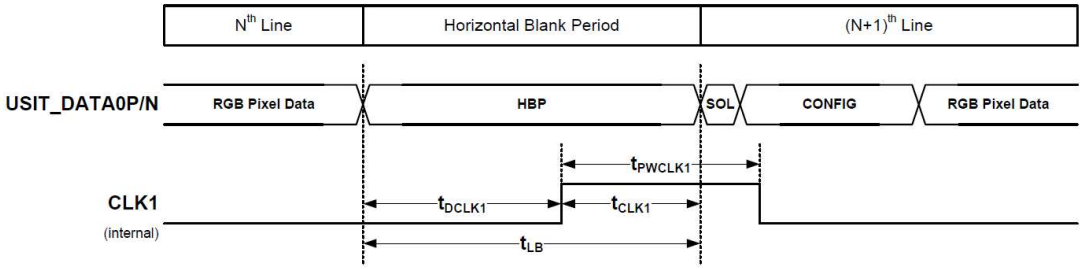


Fig.10 Timing waveform (t_{LB}, t_{CLK})

[Note6] SFC Signal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
SFC start time prior to the 1st line data	t_{START}	8	-	-	H	
SFC end time after the last line data	t_{END}	5	-	-	H	

- These timing parameters are for the vertical blank period (VBP).
- The minimum number of the VBP line is 18, including these parameters and clock training period.
- The rising and falling edge of SFC is not related to any event of the USI-T input data. In order word, SFC is an asynchronous signal to USxO/E_P/N(USIT_DATAx0_P/N).

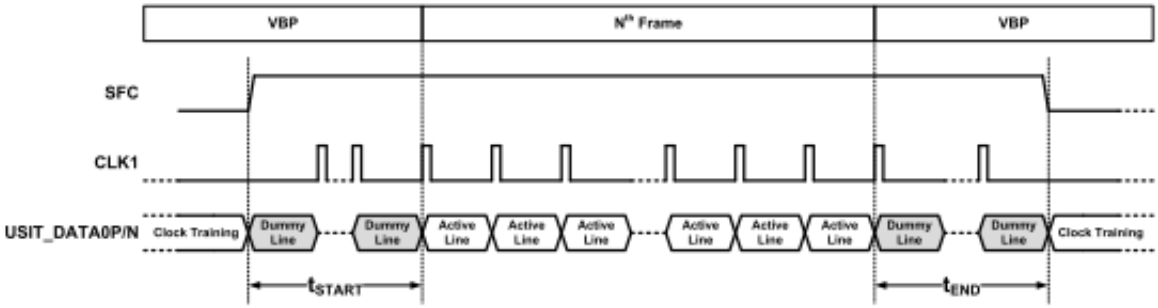


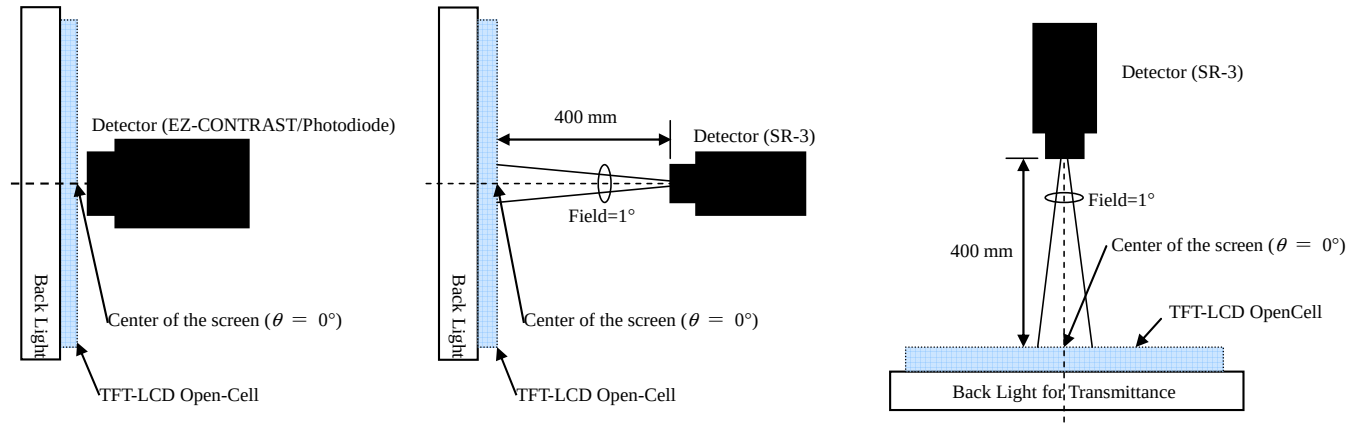
Fig.11 Timing waveform (t_{LB}, t_{CLK})

8 Optical Characteristics

Ta = 25 ºC, 60 Hz Typical Timing Input to the C-PWB

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range [1]	Horizontal	θ21 θ22	CR ≧ 10	75	89	-	deg.	
	Vertical	θ11 θ12		75	89	-	deg.	
Contrast ratio [2]		CRn	θ = 0 deg.	-	3000	-	-	
Response time [3]		τrd		-	8	-	ms	Topa=30 ºC
Chromaticity	White	Wx		Typ-0.03	0.280	Typ+0.03	-	
		Wy		Typ-0.03	0.288	Typ+0.03	-	
	Red	Rx		Typ-0.03	0.644	Typ+0.03	-	
		Ry		Typ-0.03	0.331	Typ+0.03	-	
	Green	Gx		Typ-0.03	0.300	Typ+0.03	-	
		Gy		Typ-0.03	0.604	Typ+0.03	-	
	Blue	Bx		Typ-0.03	0.151	Typ+0.03	-	
		By		Typ-0.03	0.062	Typ+0.03	-	
Transmittance [4]	White	Tr		-	5.1	-	%	
Gamma[5]		.	θ = 0 deg.	Typ-0.3	2.2	Typ+0.3		Gamma[5]

- Using the SDP Standard LED Backlight System.
- Measuring after a backlight luminance is stable.
- Measurement equipment is the following,
- Design the backlight in such a way that luminance via TFT-LCD-panel become under 420 cd/m^2 at a maximum. In case the actual luminance condition is higher than above, separate agreement has to be defined based on the evaluation result that both companies agreed.



(a). Measurement of viewing angle range and Response time.
Viewing angle range: EZ-CONTRAS
Response time: Photodiode
Gamma: CA-310

(b). Measurement of Contrast, Luminance, Chromaticity.

(c). Measurement method of panel transmittance

Fig.13 Optical measuring equipment

1) The viewing angle range is defined as the following,

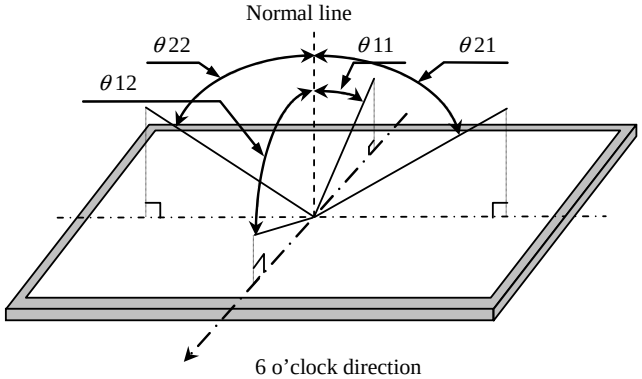


Fig.14 Measurement method of panel transmittance

2) The contrast ratio is defined as the following,

$$\text{Contrast Ratio} = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

3) The response time is defined as the following,

$$\tau_{rd} = \{\sum(\tau_r : x - y) + \sum(\tau_d : x - y)\}/20$$

τ_{rd} is an average value of a switching time from five luminance levels (0%, 25%, 50%, 75%, and 90%) to five luminance levels (0%, 25%, 50%, 75%, and 90%).

*****The following luminance level of 90% specification defines TV-signal (100IRE) level.

		Luminance level of End (y)				
		0%	25%	50%	75%	90%
Luminance level of Start (x)	0%		τ_r: 0%-25%	τ_r: 0%-50%	τ_r: 0%-75%	τ_r: 0%-90%
	25%	τ_d: 25%-0%		τ_r: 25%-50%	τ_r: 25%-75%	τ_r: 25%-90%
	50%	τ_d: 50%-0%	τ_d: 50%-25%		τ_r: 50%-75%	τ_r: 50%-90%
	75%	τ_d: 75%-0%	τ_d: 75%-25%	τ_d: 75%-50%		τ_r: 75%-90%
	90%	τ_d: 90%-0%	τ_d: 90%-25%	τ_d: 90%-50%	τ_d: 90%-75%	

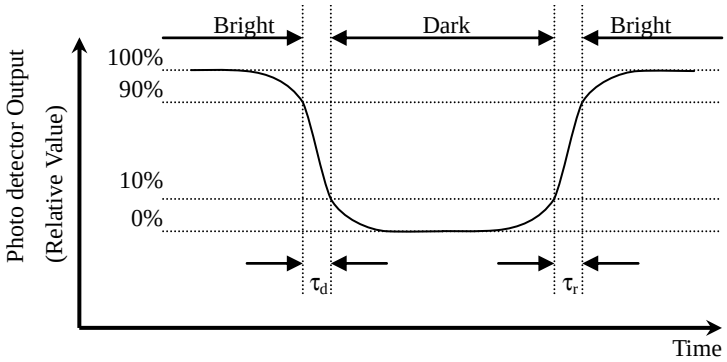


Fig.15 Definition of response time [Note]

[Note]τ_d and τ_r are defined the arrival time from 10% to 90%.

- The average value of before switching :0%
- The average value of after switching :100%

4) The transmittance is defined as the following,

$$\text{Transmittance} = \frac{\text{OpenCell luminance with all pixels white and backlight lighting}}{\text{Backlight luminance}}$$

5) This value is valid in the gradation range of V50~128/V256.

9 Shipping Specifications

9.1.Packing Form

	1-palette	1-box
Size	1815 x 1144 x 953(H) [mm]	1750 x 1085 x 145(H) [mm]
Q'ty	77 Open-Cells (7 boxes)	11 Open-Cells
Mass	About 410 kg	About 55 kg

- Refer to the attached drawing for details. (Page 19)
- This packing unit is not guaranteed other than shipment by the palette.

9.2. Label

a) Open-cell Serial Label

This label is pasted on the S-PWB. Please refer to the Open Cell Outline for the pasting area. (Page 18)

ex) JE695R3HD9KC



[Note1] How to express Lot No.

O O O O O O O O O O O

- Management Area (2-digit) [Note2]
- Suffix code (1-digit) [Note2]
- Sequence No. (5-digit)
- Production code (1-digit) [Note2]
- Production month (1~9,X,Y,Z) (1-digit)
- Production year (the last figures of the Christian Era) (1-digit)
- Serial No. (8-digit)

[Note2] Production Code & Suffix Code & Customer Code

Plant	Model No.	Production Code	Suffix Code	Customer Code	Note
Sakai	JE695R3HD9K	Z	H,M	BN96-53610A	
DG		Q	E,C,F		

※DG=DONG GUANG LCD(NANJING) CO.,LTD

▲A, ▲B

[Note3] Information in QR code (QR code:Total 38digits)

New version is introduced from Sep. 2021.

※Suffix *1~9,A~Z,"0" in case no specific code defined "Y" Last digit of the Cristian era "M"1~9,X,Y,Z "YYWW"

Size	OLB site	Production model name + Management code (1 - 14)														Lot No. (15 - 22)												SEC Part No. (26 - 31)						OLB Site (32 - 34)			Production Week (35 - 38)			
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
70"	Sakai	J	E	6	9	5	R	3	H	D	9	K	※	*	0	Y	M	Z	0	0	0	0	1	0	0	0	5	3	6	1	0	A	Z	0	2	Y	Y	W	W
	DG	J	E	6	9	5	R	3	H	D	9	K	※	*	0	Y	M	Q	0	0	0	0	1	0	0	0	5	3	6	1	0	A	Q	0	2	Y	Y	W	W

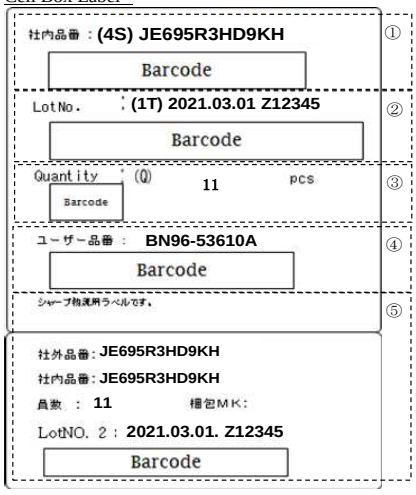
New version ▲B

Size	OLB site	Production model name + Management code (1 - 14)														Lot No. (15 - 22)											OLB Site (32 - 34)			Production Week (35 - 38)				SEC Part No. (26 - 31)					
70"	Sakai	J	E	6	9	5	R	3	H	D	9	K	※	*	0	Y	M	Z	0	0	0	0	1	0	0	0	Z	0	3	Y	Y	W	W	5	3	6	1	0	A
	DG	J	E	6	9	5	R	3	H	D	9	K	※	*	0	Y	M	Q	0	0	0	0	1	0	0	0	Q	0	3	Y	Y	W	W	5	3	6	1	0	A

b) Packing Labels

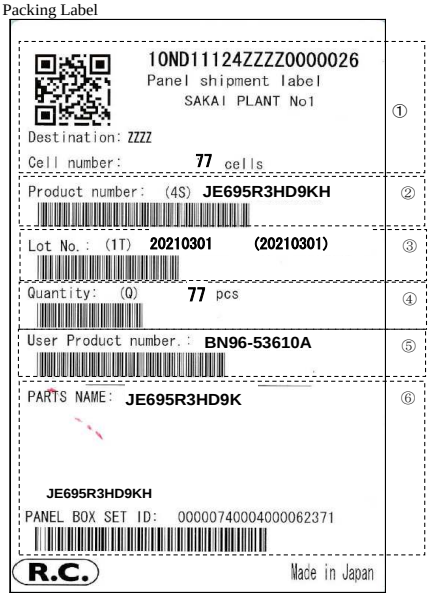
These labels are pasted on a cell box and the packing carton.

Cell Box Label



① Model No. & Suffix Code
② Lot No. (Date)
③ Quantity
④ Customer's Code
⑤ SDP Logistics Management Area

Packing Label



① Logistics Management Area
② Model No & Suffix code
③ Lot No. (Date)
④ Quantity
⑤ Customer's Code:
⑥ SDP Logistics Management Area

10 Reliability Test

No.	Test item (Test sample form)	Condition
1	High temperature storage test	Ta= 60ºC, 500h
2	Low temperature storage test	Ta= -25ºC, 500h
3	High temperature operation test	Ta= 50ºC, 500h
4	Low temperature operation test	Ta= 0ºC, 500h
5	High temperature and high humidity operation test	40ºC, 95%RH, 500hr (No condensation)
6	Heat cycle test	-20ºC, 30min ←→ 60ºC, 30min, 100cycle
7	ESD test	200pF 0Ω non-operation(contact), ±300V Charge to all terminal of S-PWB with non-operation
8	Packing Vibration test (1 Cell Box with full Open Cells)	X and Y direction: 15min, Z direction: 60min. 5Hz to 50Hz acceleration velocity: 1.0G, Sweeping ratio: 3min
9	Packing Drop test (1 Cell Box with full Open Cells)	Height: 15cm (4 sides) Number: 4 time (1 time in each of drop direction)
10	Crack test	Test criteria: 13 kgf (Push area: 15 x 15mm) * Fix the four sides of the panel in the area from the panel edge to the active area with the dedicated jig.
11	COF peeling test	COF peeling force: 1.3 kgf Peel speed:1sec/10mm

[Result evaluation criteria]

Under the display quality test condition with normal operation state, there shall be no change, which may affect practical display function.

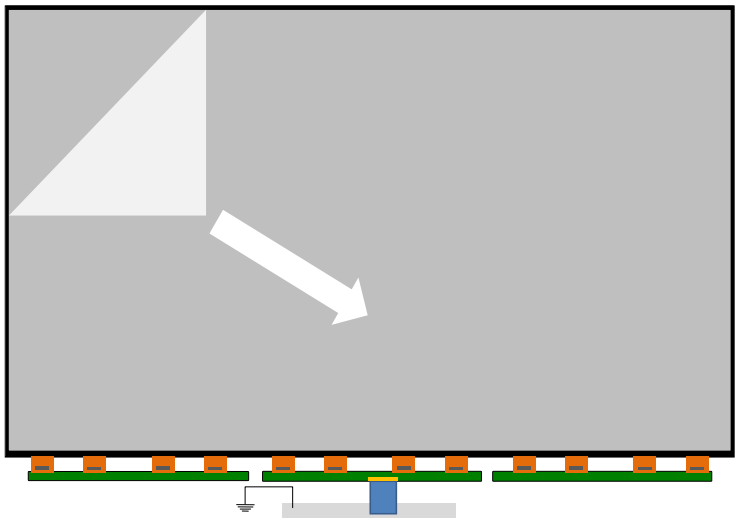
11 Precautions

a) Since this Open-Cell consists of TFTs and electronic circuits with CMOS-ICs, which are very weak to electrostatic discharges, persons who are handling the Open-Cell should be grounded through adequate methods such as the anti-static wrist band. Connector pins should not be touched directly with bare hands.

- Reference: Process control standard of SDP

	Item	Management standard value and performance standard
1	Anti-static mat (shelf)	1 to 50 [Mohm]
2	Anti-static mat (floor, desk)	1 to 100 [Mohm]
3	Ionizer	Attenuate from ±1000 V to ±100 V within 2 sec
4	Anti-static wrist band	0.8 to 10 [Mohm]
5	Anti-static wrist band entry and ground resistance	Less than 1000 ohm
6	Temperature	22 to 26 [ºC]
7	Humidity	60 to 70 [%]

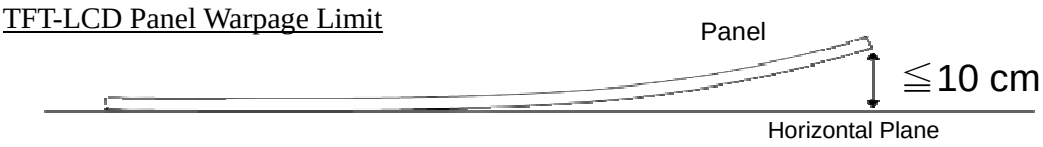
b) This Open-Cell is with the Protection Film on Polarizers. Please take care following notices within the removal of protection films.



- Be sure to peel at a constant speed.
  (The maximum peel force of this protection film is under 80gf/25mm.)
- Peeling direction shows Fig.
- Be sure to ground person with adequate methods such as the anti-static wrist band.
- Be sure to ground all terminals of the S-PWB while peeling of the protection film.
- Ionized air should be blown over during peeling action.
- The protection film must not touch drivers and S-PWBs.
- If adhesive may remain on the polarizer after the protection film peeling off, please remove with isopropyl-alcohol.

Fig.16 Direction of peeling off a protection film

c) Since the polarizer is easily damaged, pay attention not to scratch it.
d) When the polarizer is soiled, wipe it with the absorbent cotton or other soft cloth.
e) Since this TFT-LCD-panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.
f) When this TFT-LCD-panel surface gets strong pressures locally by being hit or pressed strongly by something, display Mura might remain permanently at the area where such pressures are applied. Do not push or hit by the power beyond 10N for active area of display.
g) For GOA circuit part, do not push or hit the power beyond 2.5kg/cm^2 and avoid continuous force more than 30 seconds.
h) Since the TFT is shifted a threshold with photo excitation, shade the outside of the back polarizer from the backlight.
i) There is a common electrode with the CF Glass Edge of this TFT-LCD Panel. Do not touch the CF Glass Cut Line with conductive materials since an abnormal display may occur.
j) Please don't warp or twist the TFT-LCD-panel at handling and be sure to use suction jig at handling of the Open-Cell to prevent any external damage including warpage, cosmetic dirt and scratch.

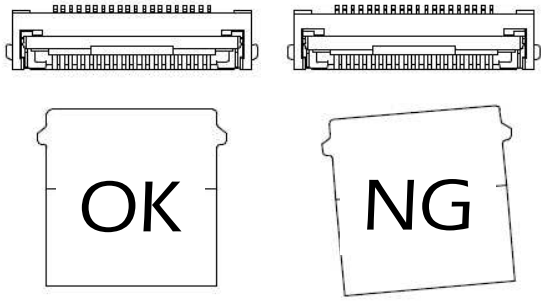


Note: This limit is only for a short time at handling of the TFT-LCD-panel.
The module and cabinets need to be designed not to add extra stress to the TFT-LCD-panel that cause warp or twist.

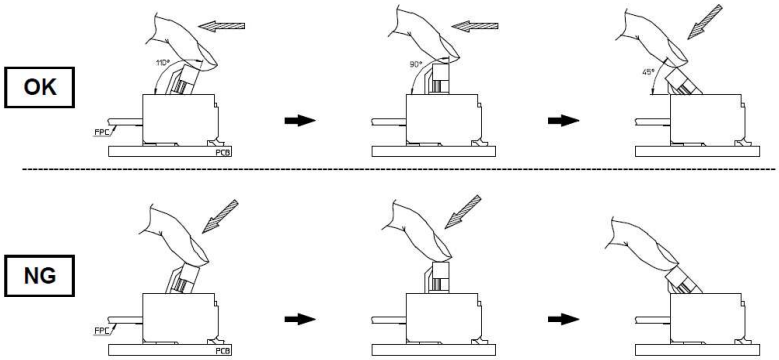
Fig.17 Limit of warpage at handling of panel

k) This Open-Cell has some PWBs, take care to keep them from any stress or pressure when handling or installing the Open-Cell, otherwise some of electronic parts on the PWB may be damaged.
l) To prevent the disconnection of S-SOFs by the thermal shock or physical damage, design the module not to fix S-PWBs with screws or tape.
m) When handling the Open-Cell and assembling them into cabinets, be noted that a long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the Open-Cell.
n) Applying too much force and stress to PWBs and SOFs may cause a malfunction electrically and mechanically.
o) In case that the SOF is needed to bend, note that the radius of bending have to be over 0.65 mm in 2 mm outside from the Driver-IC edge.
p) To radiate a heat of Source-Driver-IC(S-IC) s, the recommended operating maximum temperature is 125 ^{o}C at a chip surface, design the module to contact the opposite side of S-ICs with a high thermal conductivity material.
q) Handle with care based on the general connector's specification when inserting and removing FFCs or FPCs.
r) Since long contact with water may cause discoloration or spots, wipe off water drop immediately.
s) Turn off the power supply when inserting or disconnecting the cable.
t) This Open-Cell has high frequency circuits. Sufficient suppression to EMI should be done by system manufacturers.
u) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.
v) Since the TFT ON Mura may occur, please be careful if use 30,000h and more

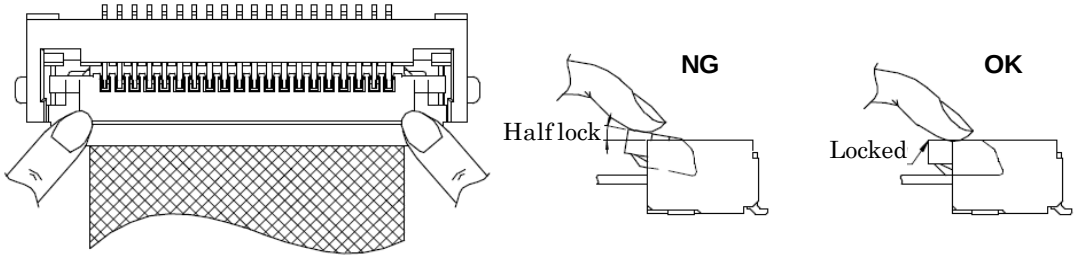
w) The chemical compound, which causes the destruction of ozone layer, is not being used.
x) Instruction of connector upon usage.
a) Do with the actuator opened completely and insert it in the interior of the insertion entrance surely Horizontally When you insert FFC or FPC. (Please put the FFC or FPC tab in the ditch of the housing surely with the FFC or FPC tab.) Might it become short defective, and it causes the corner to transform the caught terminal into the terminal by the pitch gap when inserting it right and left and diagonally.



b) Please add force in the direction where the actuator is held and do by rotating it pushing in parallel to the C-PWB direction when becoming 90°or less as shown in the figure below until the angle of the actuator becomes 90°or less when you shut the actuator. Please do not add the force to rotary axis of actuator in the direction that the actuator is off.



c) About the lock operation
When you lock, it should be push on both sides of the actuator. And it is necessary to confirm that the actuator is surely shut.



y) This Open-Cell is corresponded to RoHS. ‘‘R.C.’’ label on the side of a palette shows it.
z) Be sure to design the LCD module and cabinet not to bend the S-SOF at the unbendable area to avoid the disconnection of wires or removal of IC chip from film.
aa) In case that S-SOF are needed to bend, please note that the radius of bending have to be over 0.65 mm .

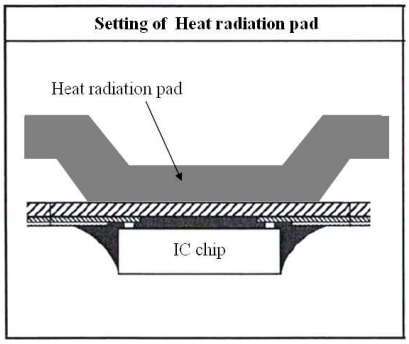


Fig.18 Diagram of setting example of heat radiation pad on S-SOF

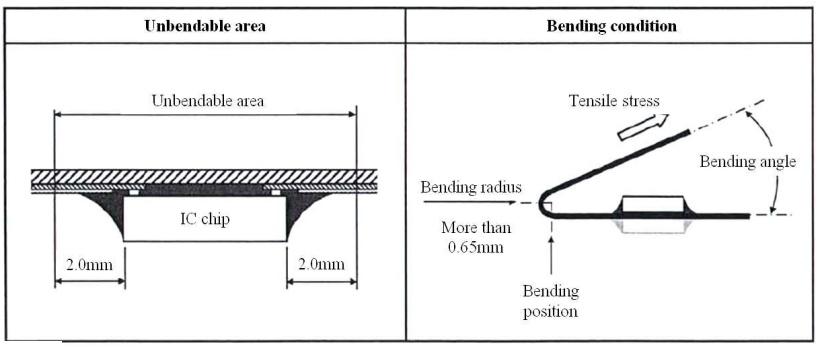


Fig.19 Unbendable area and Bending condition of S-SOF

bb) Be sure to design the LCD module and cabinet not to fix with SPWB by screws to prevent the disconnection of S-SOF by the thermal shock or physical damage.
cc) When the panel surface gets the strong pressure locally by being hit or pressed strongly by something, display Mura might remain permanently at the area where such pressure is applied. Therefore, please be careful well of handling panel in your production process and also call end customer attention for careful handling.
dd) Since damage may be done from the sticker within permission, please do not use the corner edge of a panel for positioning use or holding a panel.
ee) Since there is possibility of injury with the panel edge, please design the TV set so that the user can not touch the panel edge.
ff) When any question or issue occurs, it shall be solved by mutual discussion.

12 Storage Conditions of Open-Cell in Cell-Box

Temperature	0°C to 40°C
Humidity	95% RH or less
Reference condition	20°C to 35°C, 85% RH or less (summer) 5°C to 15°C, 85% RH or less (winter) The total storage time (40°C, 95% RH) :240 hours or less
Sunlight	Shelter a production from the direct sunlight.
Atmosphere	Harmful gas, such as acid and alkali which bites electronic components and/or wires must not be detected.
Notes	Put the box on a palette or a base, do not put it on a floor, and store them with removing from a wall. Take care of ventilation in storehouse and around cartons, and control changing temperature is within limits of natural environment.
Storage life	1 year

SDP Confidential

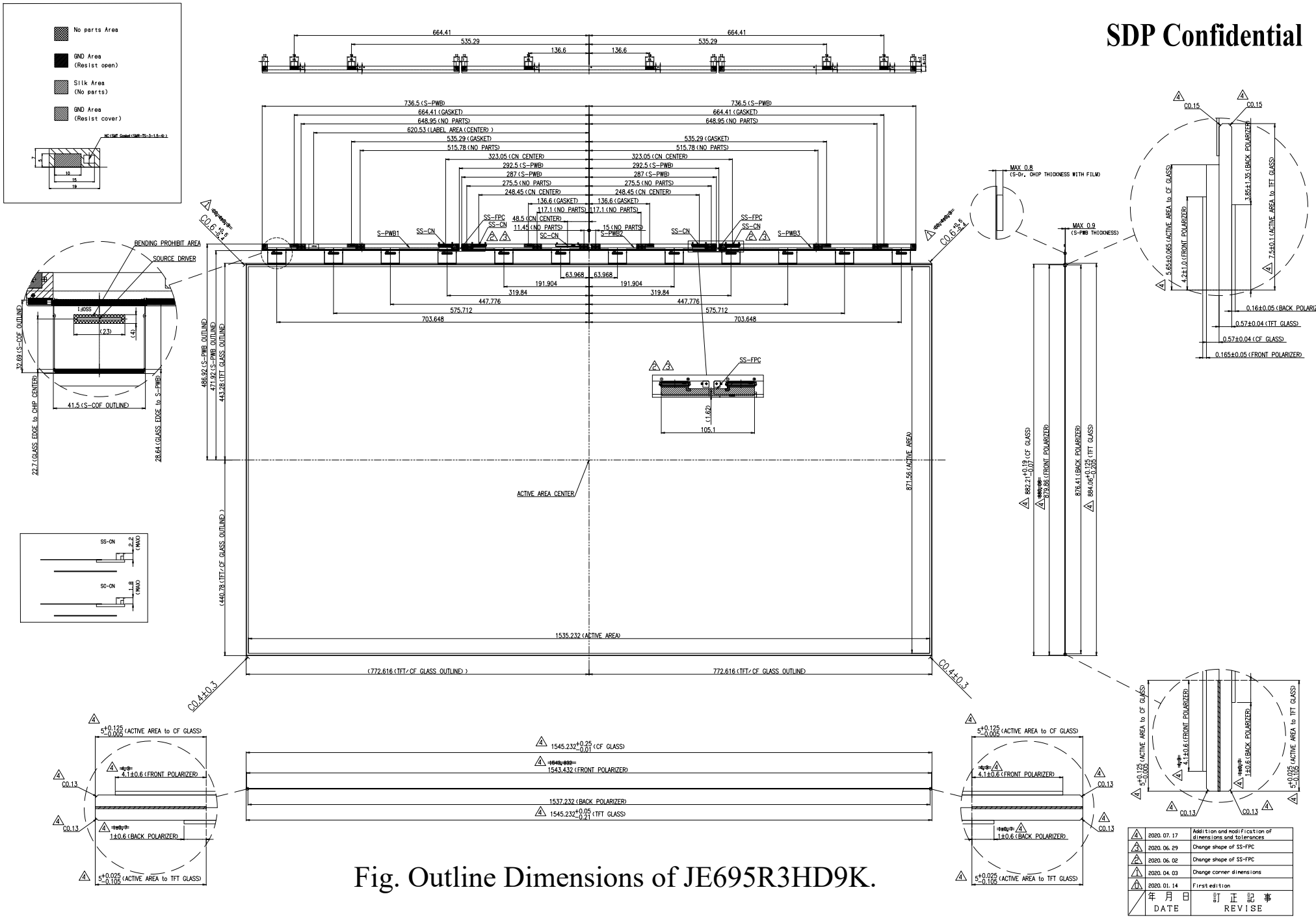


Fig. Outline Dimensions of JE695R3HD9K.

4	2020. 07. 17	Addition and modification of dimensions and tolerances
3	2020. 06. 29	Change shape of SS-FPC
2	2020. 06. 02	Change shape of SS-FPC
1	2020. 04. 03	Change corner dimensions
0	2020. 01. 14	First edition
	年 月 日 DATE	訂 正 記 事 REVISE

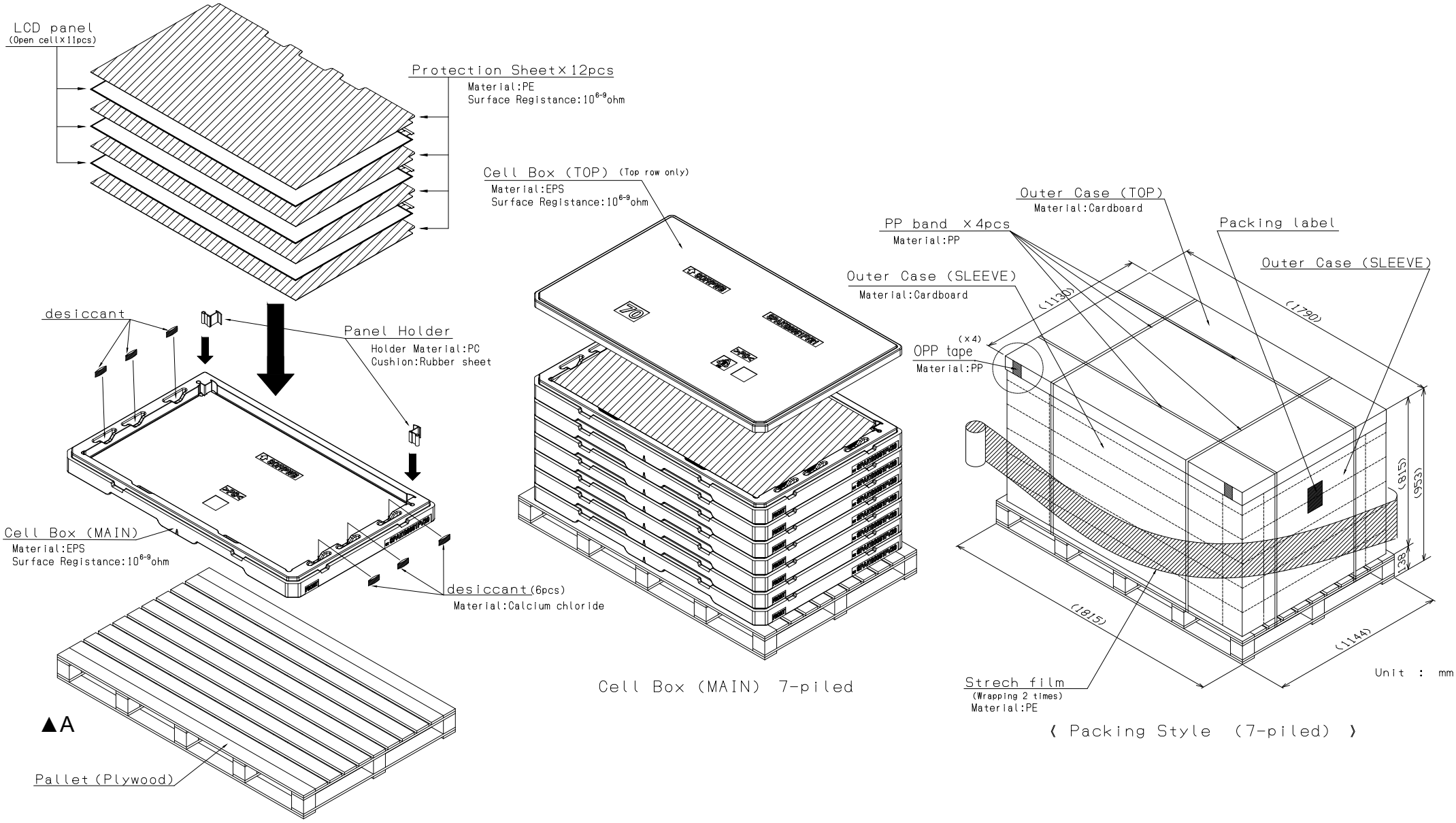


Fig. JE695R3HD9K Packing Form

▲A