Model name: PT430CT03-14

Product Specification

Rev.F7

( ) Preliminary Specification

(√) Final Specification

Any modification is not allowed without HKC's permission

Customer's Approval	**MianYang HKC**
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Revision History

Version	Date	Page (New)	Section	Description	Revision by
Pre. 1.0	2020/1/17	-	All	Preliminary Specification was first issued.	
Rev. F1	2020/7/17		All	Power On/Off Sequence	Fantao
Rev. F2	2020/9/17	5	2.2	Panel Surface Temperature of Display Area	Liu Jinxin
Rev. F3	2020/9/30	11	3.2.2	LVDS interface Connector Drawing	Yuan zhenghui
Rev. F4	2020/10/12	15	3.4	Power On/Off Sequence	Yuan zhenghui
Rev. F5	2020/10/20	7	3.1.2	LVDS characteristics common input voltage	Yuan zhenghui
Rev. F6	2020/10/29	15	3.4	Power On/Off Sequence	Yuan zhenghui
Rev. F7	2020/12/01	19	4.2	Update Color Chromaticity, Color Gamut	Zheng Xinglong
Rev.F7	2020/12/07	21	4.2	Update the gamma scale	Yuan zhenghui
Rev. F7	2020/12/08	23	5.2.1	Update Pallet＆Pallet after Packing Dimensions	Yang xiaohui
		24	6	Update Label	
		25	6.3	Update Pallet Label	
Rev. F7	2021/07/07	23	5.2	Update Packing	Zhao Zhilong

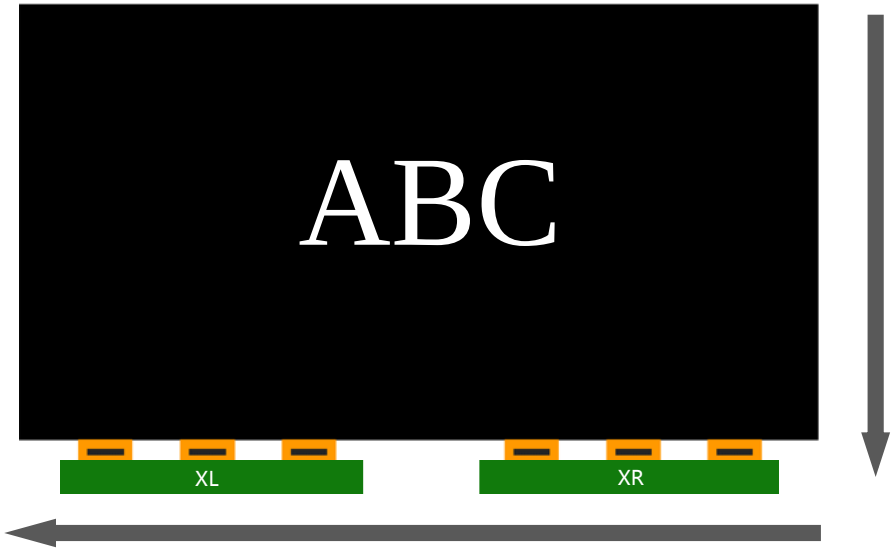
1. GENERAL DESCRIPTION

The specification is applied to 43” model (PT430CT03-14) TFT Liquid Crystal Display open cell and it supports 1920 x 1080 FHD mode with 16.78M (8bit) colors. This product is with data driver ICs and two 68-pins connectors withmini-LVDS interface on each left and right S-PCB without built-in backlight unit.

1.1 General Specifications

Item	Specification	Unit	Note
Screen Size	43	inch	-
Cell Outline Dimension	950.896(H)x 541.750(V) x1.4(D)(Typ.)	mm	
Active Area	940.896(H) x 529.254(V)	mm	
Driver Element	a-Si TFT active matrix	-	-
Cell Transmittance	6.3%	-	Center point
Pixel Number	1920 x 1080	pixel	-
Pixel Pitch	490.05(H) x 490.05(V)	um	-
Pixel Arrangement	RGB vertical	-	-
Display Colors	16.78M	color	8 Bit
Display Mode	Normally Black	-	-
Display Orientation	Signal input with “ABC”	-	(1)
Surface Treatment	Treatment: AG	-	-
	Hardness:3H		-
	Haze:3%	-	-
Weight	1.6(Typ.)	Kg	

Note (1):



2. ABSOLUTE MAXIMUM RATINGS

2.1 Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause damage to the unit.

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	13.5	V	(1)
Input Signal Voltage	V_{in}	-0.3	3.6	V	(1)

Note:

(1) Within Ta=25±2℃

2.2 Absolute Ratings of Environment

Temperature and relative humidity range is shown in the figure below.

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	60	℃	(1)
Operating Temperature	TOP	0	50	℃	(1), (2)
Panel Surface Temperature of Display Area	PST	-	65	℃	(3)

Note:

(1) a. 90 % RH Max. (Ta ≤ 40 °C).

b. Web-bulb temperature should be 39℃ Max.(Ta>40℃)

c. No condensation

d. Operating condition with a assemble module

(2) Any point on the Driver surface must be less than 120 ℃ under any condition ,If the surface temperature is out of the spec, thermal solutions should be applied to avoid be damaged.

(3) Surface temperature of display area is measured at 50℃ dry condition.

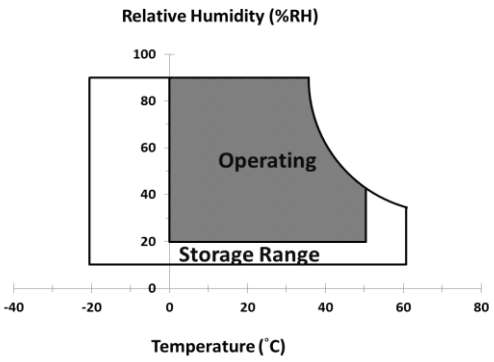


Fig. 2.1 Operating and Storage Environment

2.3 Package Storage

When storing open cell as spares for a long time, please follow the precaution instructions:

(1) Do not store the open cell in high temperature and high humidity for a long time. It is highly recommended to store the module with temperature from20℃ to 30℃in normal humidity (50 ±10%RH) with shipping package.

(2) The open cell should be keep within one month shelf life.

3. ELECTRICAL SPECIFICATIONS

3.1 Electrical Characteristics

3.1.1 Power Consumption(Ta = 25 ±2 ℃)(1)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCC	10.8	12.0	13.2	V	(2)
Rush Current		IRUSH	-	-	3.0	A	(3)
Power Supply Current	White Pattern	ICC		0.27	0.30	A	(4)
	Horizontal Stripe	ICC		0.45	0.48	A	
	Mosaic 7×5	ICC		0.27	0.30	A	
Power Consumption		P_{LCD}		3.6	5.76	W	

Note:

(1)Ambient temperature: 25 ±2℃

(2)The ripple voltage should be controlled under 10% of VCC.

(3)Measurement Conditions: VCC rising time=470μs.

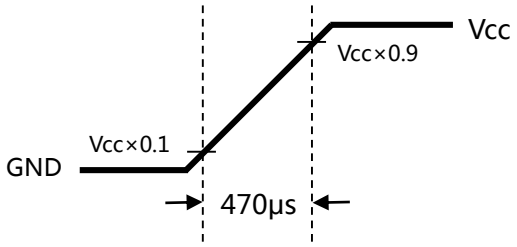


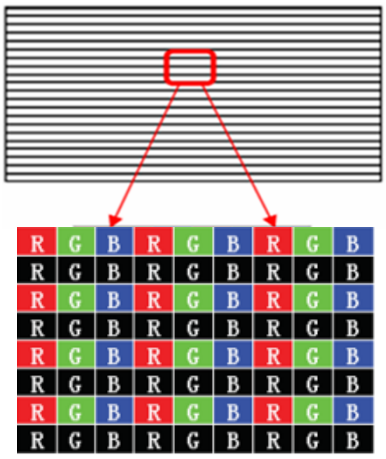
Fig 3.1 V_{CC} rising time condition

(4) a. Measurement Conditions: Vcc =12V, Ta = 25 ±2 ℃, F = 60 Hz, whereas the test pattern is shown as below.

A. White Pattern



B. Horizontal Strip



C. Mosaic Pattern

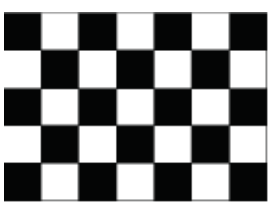


Fig 3.2 Test patterns

b. The typcal power consumption is specified with theMosaic 7×5 Pattern.

c. The max power consumption is specified with the Horizontal Strip Pattern.

3.1.2 LVDS characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
LVDS interface	Differential Input High Threshold Voltage	V_{TH}	+100	-	-	mV	(1)
	Differential Input Low Threshold Voltage	V_{TL}	-	-	-100	mV	
	Common Input Voltage	VCM	1	1.2	1.4	V	
	Differential Input Voltage	|VID|	100	-	600	mV	
	Terminating Resistor	RT	80	100	120	ohm	
CMOS interface	Input High Threshold Voltage	VIH	3	3.3	3.6	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.6	V	

Note:

(1) The LVDS input signal has been defined as follows:

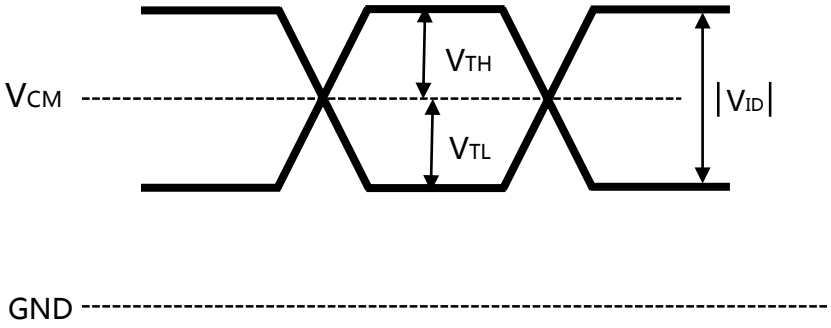


Fig 3.3 LVDS input signal

3.1.3 LVDS format

VESA Format: SEL_LVDS=H

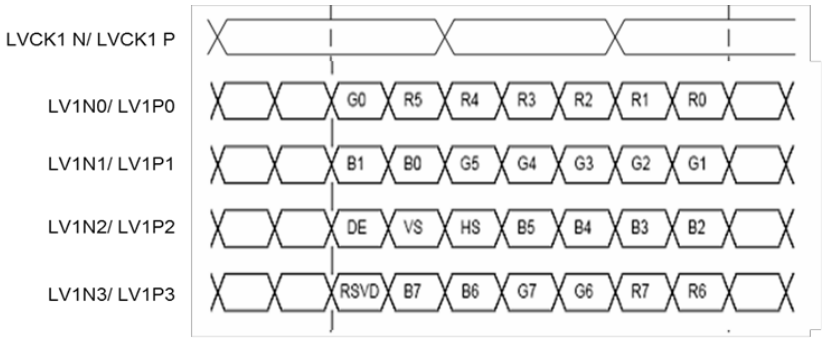


Fig 3.4 VESA format

JEIDA Format: SEL_LVDS = L or Open

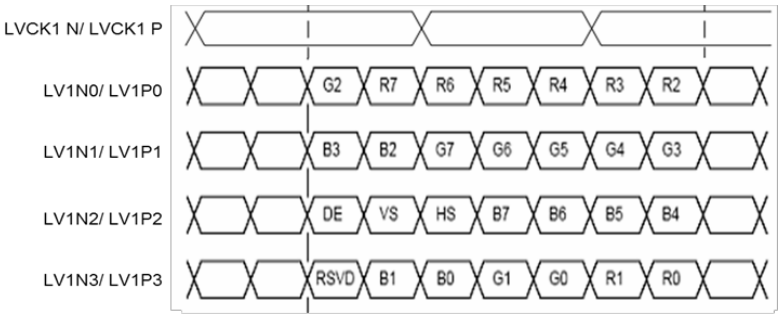


Fig 3.5 JEIDA format

3.1.4 Block diagram

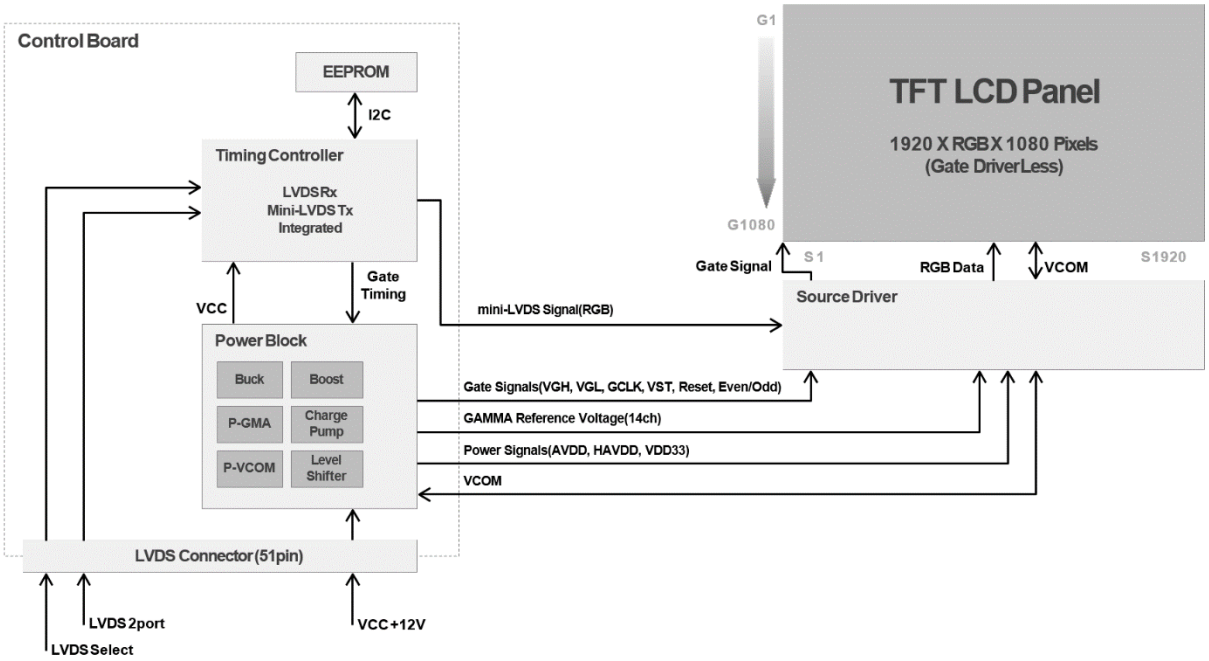


Fig 3.6 Block diagram

3.2 Interface Connections

3.2.1 Interface Pin Assignment

Connector part No. : CN1 FFC/21EJ0-104-0004 (JONHON) (or compatible type) (1)

PinNo.	Symbol	Description	Note
1	WP	Write Protection	(2)
2	SCL	I2CClock	
3	SDA	I2CData	
4	NC	No connection	
5	NC	No connection	
6	NC	No connection	
7	LVDS_SEL	LVDS data format selection	(3)
8	NC	No connection	
9	BIST_MODE	Select BIST Mode	(4)
10	NC	No connection	
11	GND	Ground	
12	LV1N0	LVDS Channel 1,Signal0-	
13	LV1P0	LVDS Channel 1,Signal0+	
14	LV1N1	LVDS Channel 1,Signal1-	
15	LV1P1	LVDS Channel 1,Signal1+	
16	LV1N2	LVDS Channel 1,Signal2-	
17	LV1P2	LVDS Channel 1,Signal2+	
18	GND	Ground	
19	LV1CLKN	LVDS Channel1,Clock-	
20	LV1CLKP	LVDS Channel1,Clock+	
21	GND	Ground	
22	LV1N3	LVDS Channel 1,Signal3-	
23	LV1P3	LVDS Channel 1,Signal3+	
24	NC	No connection	
25	NC	No connection	
26	NC	No connection	
27	NC	No connection	
28	LV2N0	LVDS Channel 2,Signal0-	
29	LV2P0	LVDS Channel 2,Signal0+	
30	LV2N1	LVDS Channel 2,Signal1-	
31	LV2P1	LVDS Channel 2,Signal1+	

32	LV2N2	LVDS Channel 2,Signal2-	
33	LV2P2	LVDS Channel 2,Signal2+	
34	GND	Ground	
35	LV2CLKN	LVDS Channel2,Clock-	
36	LV2CLKP	LVDS Channel2,Clock+	
37	GND	Ground	
38	LV2N3	LVDS Channel 2,Signal3-	
39	LV2P3	LVDS Channel 2,Signal3+	
40	NC	Noconnection	
41	NC	Noconnection	
42	NC	Noconnection	
43	NC	Noconnection	
44	NC	Noconnection	
45	GND	Ground	
46	GND	Ground	
47	NC	Noconnection	
48	VDD	Power Supply Input Voltage(+12V)	
49	VDD	Power Supply Input Voltage(+12V)	
50	VDD	Power Supply Input Voltage(+12V)	
51	VDD	Power Supply Input Voltage(+12V)	

Note:

(1) Following finger shows the LVDS pin1diagram

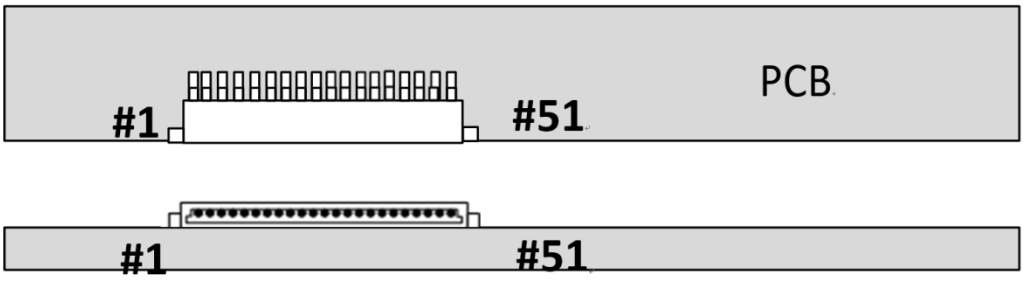


Fig 3.7 LVDS connector direction sketchmap

(2) WP pull high/lowsetting

L = Connect to GND, H =Connect to +3.3V

WP	Note
L or Open	Write Disable
H	Write Enable

(3) LVDS_SEL pull high/low setting

L = Connect to GND, H =Connect to+3.3V

LVDS_SEL	Note
H	VESA
L orOpen	JEIDA

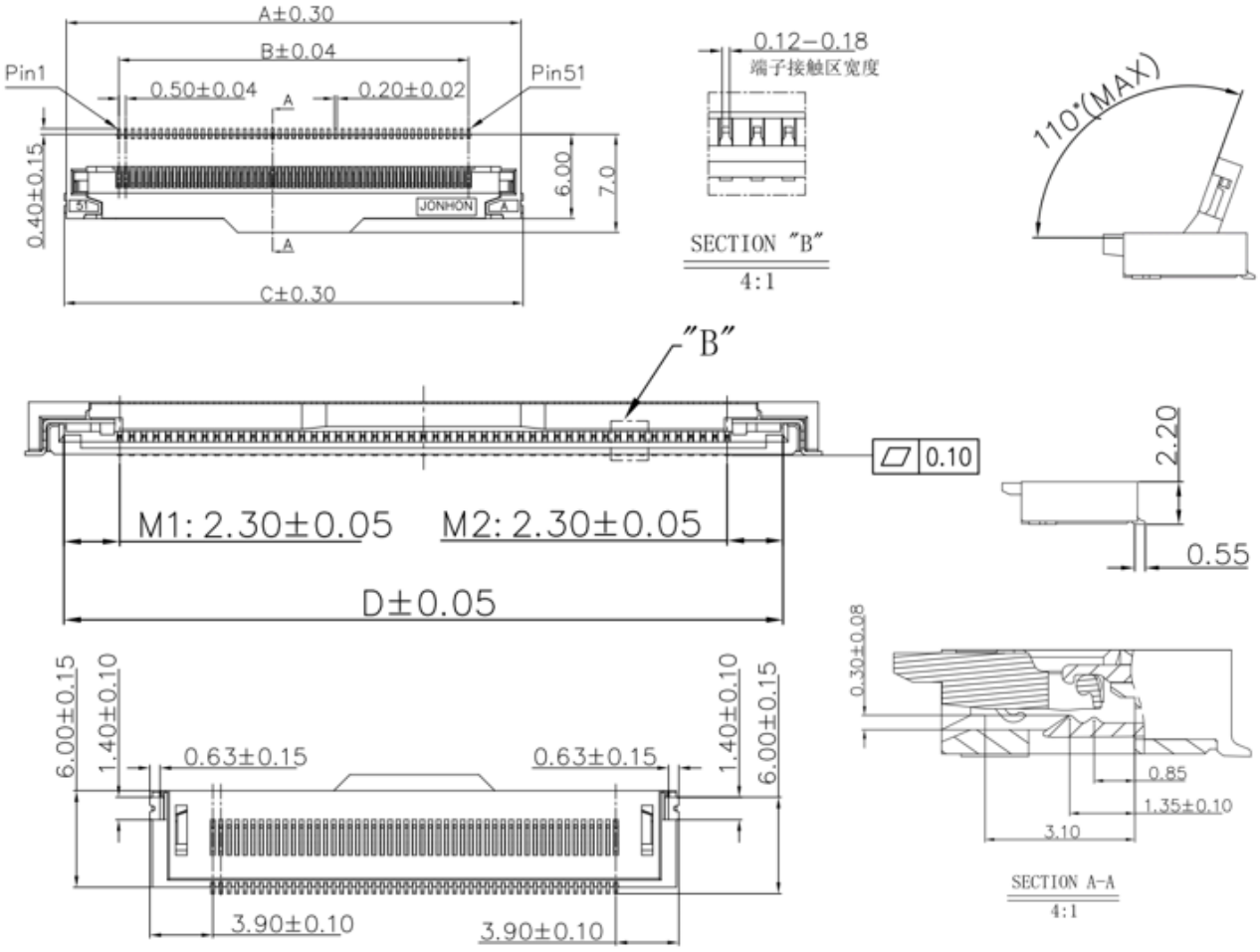
(4) BIST_MODE pull high/low setting

L = Connect to GND, H =Connect to+3.3V

BIST_MODE	Note
L or Open	Available LVDS Signal input:Display LVDS Input Pattern No LVDS Signal or unavailable LVDS Signal input: Display Black Pattern
H	Available LVDS Signal input:Display LVDS Input Pattern No LVDS Signal or unavailable LVDS Signal input: Display Bist Pattern

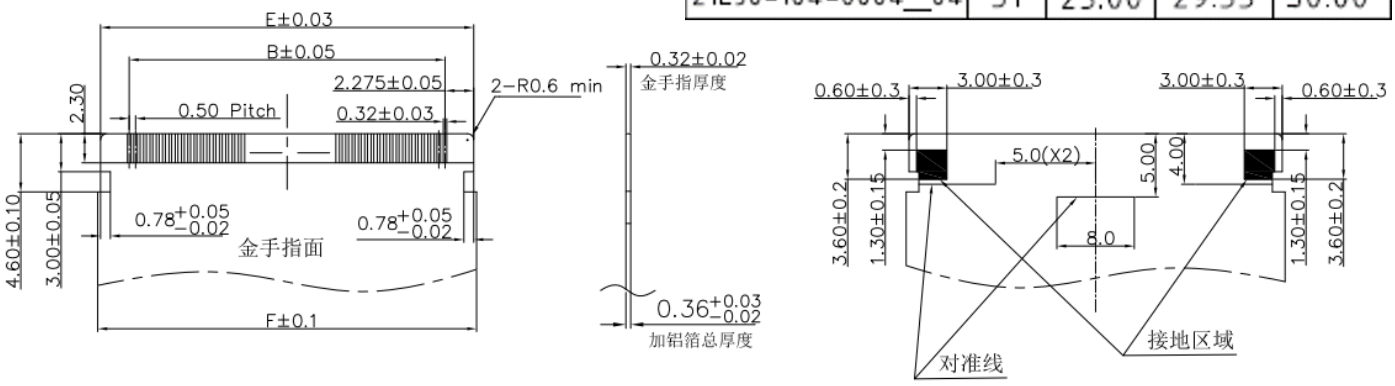
3.2.2Connector Drawing

Input LVDS Interface 51PIN



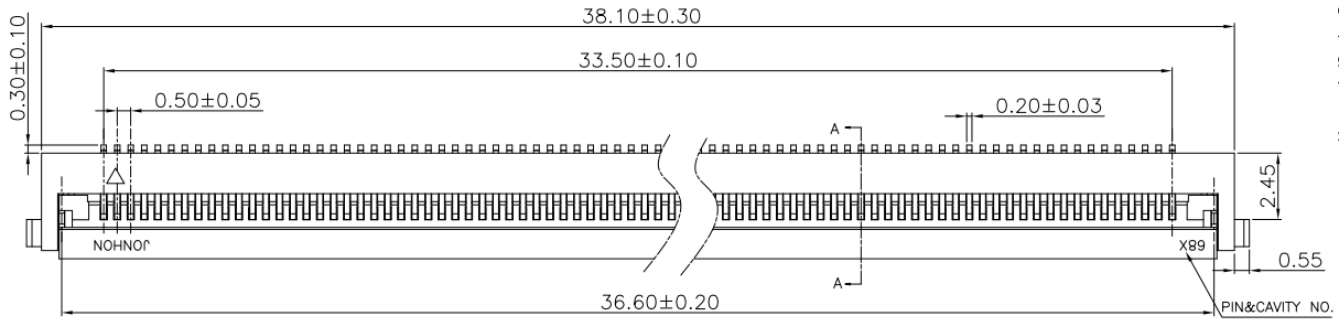
P/N	PIN	DIM:A	DIM:B	DIM:C	DIM:D
21EJ0-104-0004__04	51	32.64	25.00	32.80	29.60

P/N	PIN	DIM:B	DIM:E	DIM:F
21EJ0-104-0004__04	51	25.00	29.55	30.00

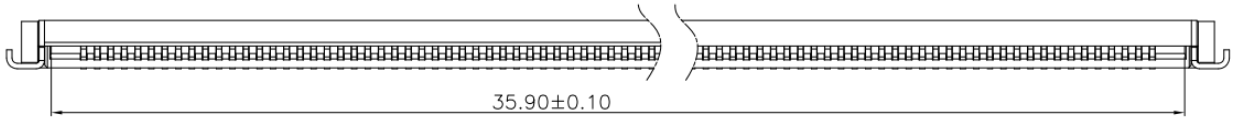


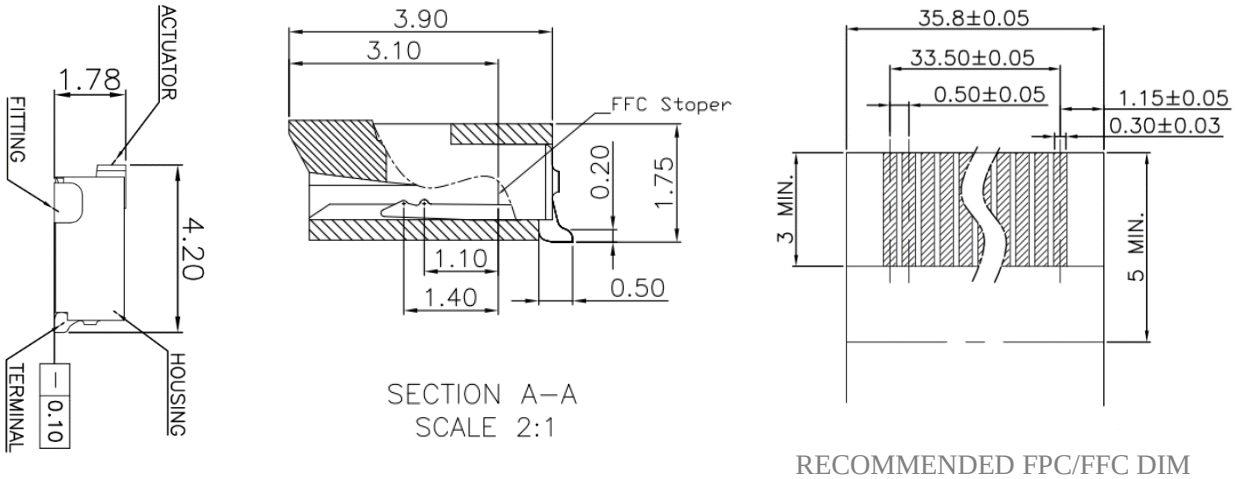
APPLICABLE FPC RECOMMENDED DIMENSION

Mini-LVDS Interface 68PIN



21EJ0-100-0005_04/JONHON





RECOMMENDED FPC/FFC DIM

THICKNESS:0.3±0.03

Fig 3.8 Connector and FFC

3.3 Timing Spec

The input signal timing specifications are shown as the following table and timingdiagram

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	**F_{clkin}**	65	74.25	78	MHz	（1）
	Input cycle to cycle jitter	Trcl	10	—	200	ps	（2）
	Spreadspectrumm	Fclkin_mod	Fclkin-2%	—	Fclkin+2%	MHz	（3）
	Spread spectrum modulationfreque	FSSM	10	—	200	KHz	
LVDS Receiver	Margin	TRSM	-380	—	380	ps	(4)
Vertical Term	Frame Rate	**F**	48	60	70	Hz	
	Total	**T_V**	1115	1125	1500	T_H	$T_V = T_{VD} + T_{VB}$
	Active Display	**T_{VD}**		1080			
	Blank	**T_{VB}**	35	45	420	T_H	
Horizontal Term	Total	**T_H**	1075	1100	1580	T_{CLK}	$T_H = T_{HD} + T_{HB}$
	Active Display	**T_{HD}**		960			
	Blank	**T_{HB}**	115	140	620	T_{CLK}	

Attention:

The module is operated in DE only mode, Hsync and V sync input signal have no effect on normal operation.

Note:

（1）Please make sure the range of pixel clock follows the following equations:

$$F_{CLK}(max) \geq F_{max} \times T_V \times T_H \qquad F_{CLK}(min) \leq F_{min} \times T_V \times T_H$$

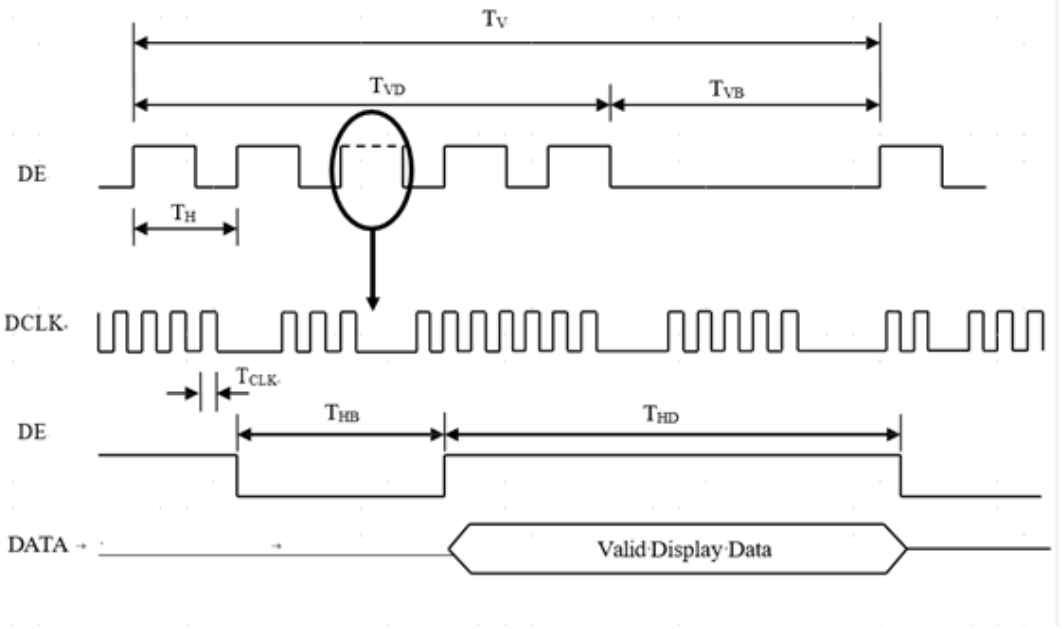


Fig 3.9 Signal timing diagram

（2）The input clock cycle-to-cycle is defined as below figures.

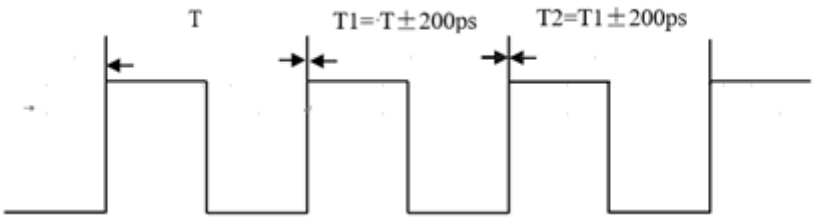


Fig 3.10Jitter

（3）The SSCG (Spread Spectrum Clock Generator) is defined as the following figure.

The LVDS SSM's suggestion is off by default, SOC board must test all validation if SOC board open the LVDS SSM

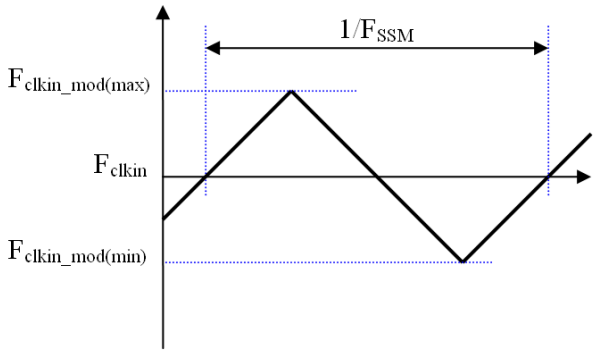


Fig 3.11SSCG

The LVDS timing diagram and setup/hold time is defined and showed as the following figure.

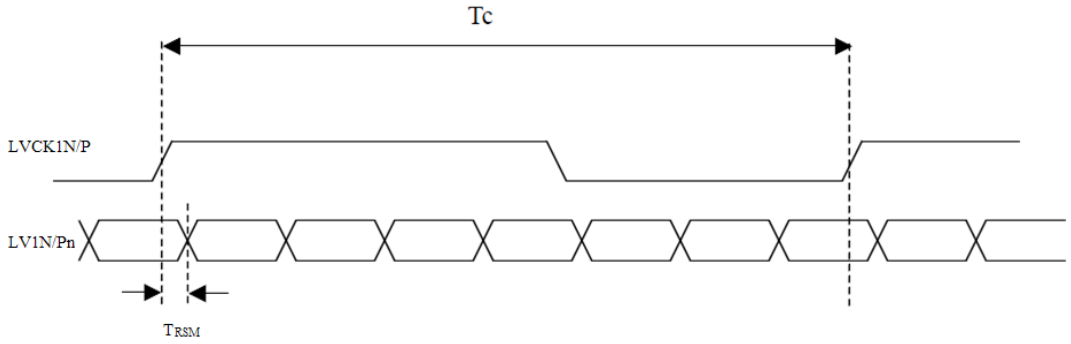


Fig 3.12LVDS receive interface timing diagram

3.4 Power On/Off Sequence

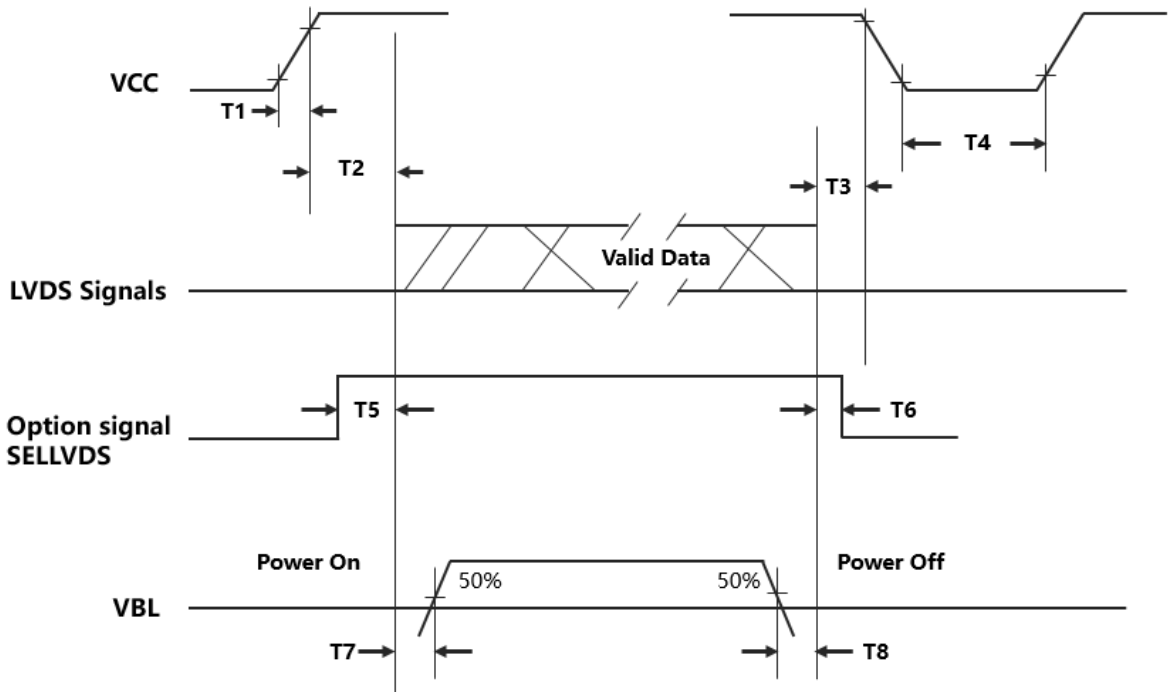


Fig 3.13 Power on/off

	Min.	Typ.	Max.	
T1	0.4	-	10	ms
T2	10	-	200	ms
T3	10	-	200	ms
T4	1000	-	-	ms
T5	-	-	T2	ms
T6	-	-	T3	ms
T7	500	-	-	ms
T8	200	-	-	ms

Attention :

(1)The supply voltage of the external system for the module input should be the same as the definition.

(2) To avoid some abnormal display noise, we suggest " VCC falling time" to follow "T8" definition.

(3) The product should be always operated within above ranges.

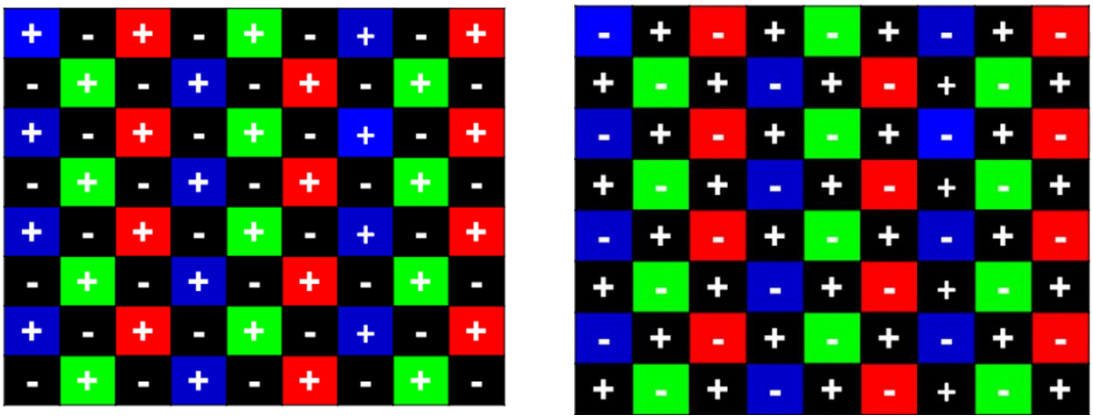
(4) In case of VCC is off level, please keep the level of input signals on the low or keep high impedance.

3.5 Flicker Adjustment

Flicker must be optimized after module assembly and aging. Its patterns are as follow:

sub pixel checker under 50% gray level

Sub pixel checker 128 gray



Frame　　Frame N+1

3.14 Bright sub-pixel=G127(50% grayscale); dark sub-pixel=G0（0% grayscale）

3.6 Driver IC ESD Spec

If the LCD module is designed with the Plastic Bezel, we suggest ESD protection solutions should be applied to avoid IC damaged, as shown in Fig 3.15

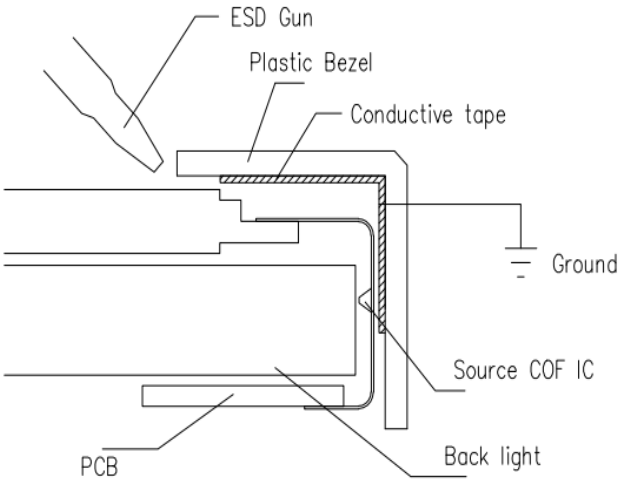


Fig 3.15 Source COF IC ESD protection

4. OPTICAL CHARACTERISTICS

4.1 Measurement Conditions

The table below is the test condition of optical measurement.

Item	Symbol	Value	Unit
Ambient Temperature	T_A	25±2	℃
Ambient Humidity	H_A	50±10	%RH
Supply Voltage	V_{CC}	12	V
Driving Signal	Refer to the typical value in Chapter 3: Electrical Specification		
Vertical Refresh Rate	F_v	60	Hz
Light source	HKC Backlight module White LED Backlight Module/ Film structure		
Warm up time	Twarm	>30 min	min
Dark room	ED	1lux>	lux

To avoid abrupt temperature change during optical measurement, the measurement should be executed in a stable, windless, in dark room after lighting the light source.

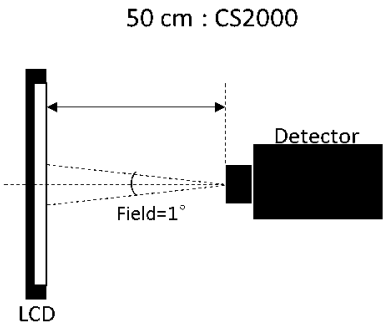


Fig 4.1 Measurement equipment.

4.2 Optical Specifications

The relative measurement methods of optical characteristics are shown in 4.2. The following items should be measured under the test conditions described in 4.1 and stable environment shown in 4.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity (CIE1931)	Red	Rx	θ_x=0°,θ_y=0 ° Viewing Angle at Normal Direction at center point of panel, Light source is HKC Backlight	Typ. - 0.03	0.640	Typ. + 0.03	--	(1)
		Ry			0.336			
	Green	Gx			0.306			
		Gy			0.606			
	Blue	Bx			0.151			
		By			0.057			
	White	Wx			0.287			
		Wy			0.308			
Color Gamut		CG		70	71		%	(2)
Transmittance		T%		5.9	6.3		%	(3)
Contrast Ratio		CR	θ_x=0°,θ_y=0 °	1000	1200		-	(4)
Response Time		T_g		-	8	10	ms	(5)
Viewing Angle	Horizontal	θ_x+	CR≧10 θ_x=0°,θ_y=0 °	-	89	-	Deg.	(6)
		θ_x-		-	89	-		
	Vertical	θ_y+		-	89	-		
		θ_y-		-	89	-		
Cross talk (2D)		CT		-	-	2	%	(7)
Gamma		γ		2.0	2.2	2.4	-	(8)

Note:

(1) Each chromaticity coordinates (x, y) are measured in CIE1931 color space when full-screen displaying (Red, Green, Blue, White) and light source is defined by HKC Backlight, measurements shall be made at the center of the panel, and setup of measurement is shown in Fig 4.1.

(2) The color gamut is defined as the fraction in percent of the area of the triangle bounded by R, G, B coordinates and the area is defined by NTSC 1931 color standard in the CIE color space. Chromaticity coordinates are measured by CS2000 and the standard setup of measurement is shown in Fig 4.1.

(3) Definition of Transmittance (T%):

The transmittance is measured with full white pattern (L_{max}) at the center of the LCD panel.

$$\text{Transmittance (T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}}$$

(4) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression,

Contrast Ratio (CR): $\boldsymbol{CR} = \frac{\boldsymbol{CR_W}}{\boldsymbol{CR_D}}$

CR_W : Luminance of LCD module with full screen white pattern (255,255, 255) at center point.

CR_D : Luminance of LCD module with full screen Dark pattern (0, 0, 0) at center point.

Where the measure point of to the Contrast Ratio is the center of the panel

(5) Definition of Response time (Tg):

Average of gray to gray response time (T_g) means the average switching time of luminance ratios among 0%,25%,50%,75%,and 100% to each other and is optimized on frame rate =60Hz.

Measured Response time		To				
		0%	25%	50%	75%	100%
From	0%		$T_{0\%to25\%}$	$T_{0\% to 50\%}$	$T_{0\% to 75\%}$	$T_{0\% to 100\%}$
	25%	$T_{25\% to 0\%}$		$T_{25\% to 50\%}$	$T_{25\% to 75\%}$	$T_{25\% to 100\%}$
	50%	$T_{50\% to 0\%}$	$T_{50\% to 25\%}$		$T_{50\% to 75\%}$	$T_{50\% to 100\%}$
	75%	$T_{75\% to 0\%}$	$T_{75\% to 25\%}$	$T_{75\% to 50\%}$		$T_{75\% to 100\%}$
	100%	$T_{100\% to 0\%}$	$T_{100\% to 0\%}$	$T_{100\% to 50\%}$	$T_{100\% to 75\%}$	

Table 4.2 Switching time of luminance ratios matrix

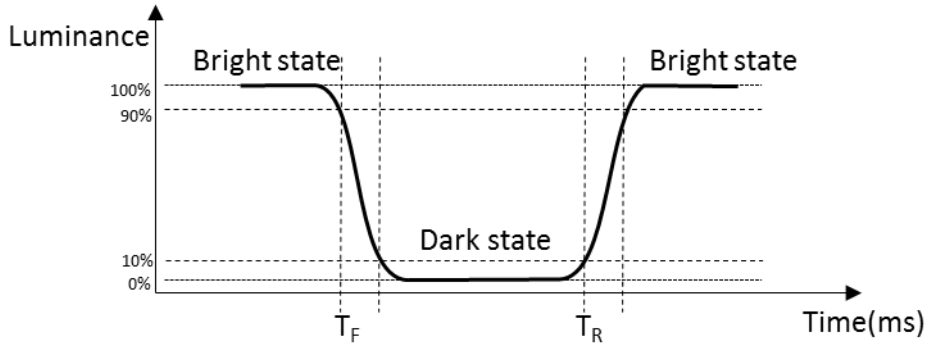


Fig 4.3 The definition of TR and TF

Measured response time is determined by 10% to 90% brightness difference of rising (T_R) or falling (T_F) time.

(6) Definition of Viewing angle:

As Note (4) the static contrast ratio definition, the viewing angles are defined at the angle that the contrast ratio is larger than 10 at four directions relative to the perpendicular direction of the HKC's module (two vertical angles: up θ_y+ and down θ_y-; and two horizontal angles: right θ_x+ and left θ_x-). The standard setup of measurement is shown in Fig 4.1 & 4.4

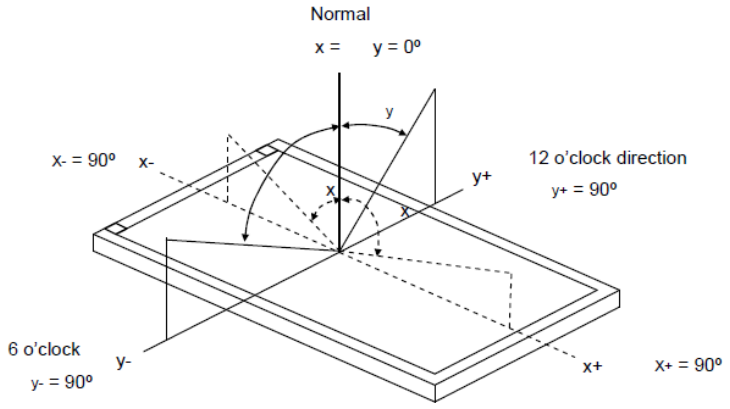


Fig 4.4 Definition of Viewing angle

(7) Definition of Crosstalk (2D)

Crosstalk of one area of the LCD surface by another shall be measured by comparing the luminance (A), with all display pixels set to a gray level, to the luminance (B) of that same area when any adjacent area is driven full white pattern which shown in Fig. 4.5. The gray level of background is set to 25%full gray pattern.

$\text{Crosstalk}(\%) = \text{Max.}\left(\frac{|L_B(\text{X}) - L_A(X)|}{L_A(X)} \times 100\%\right)$, Where the X is point 1 to 4 shown in Fig.4.5

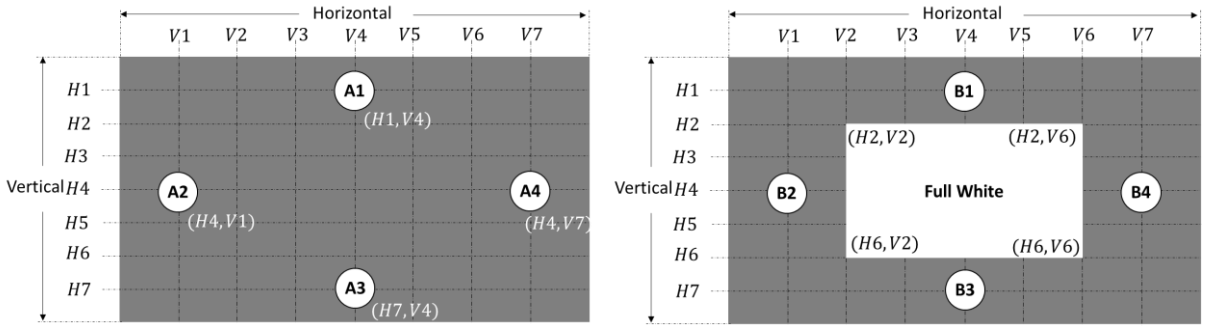


Fig 4.5 Definition of Crosstalk (2D)

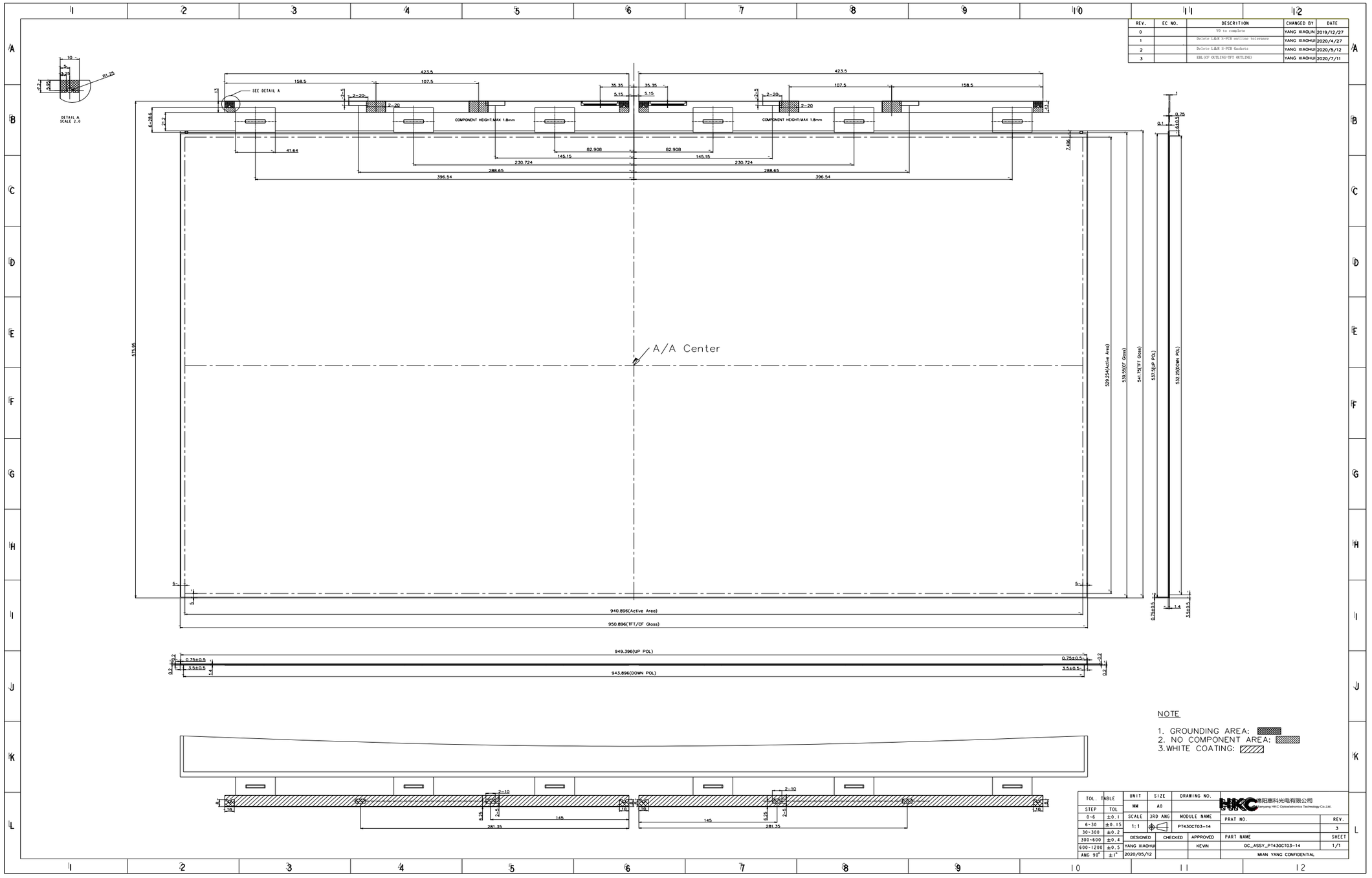
(8) The gamma scale is calculated with below equation

Gamma Scale= Each center gamma value of gray level (G.L) between 31 and 223.

$$\text{local gamma}(\text{G.L.}) = Log_{\frac{G.L.}{255}}\left(\frac{Luminance(G.L.)}{Luminance(L255)}\right)$$

5. MECHANICAL CHARACTERISTICS

5.1 Mechanical Specification



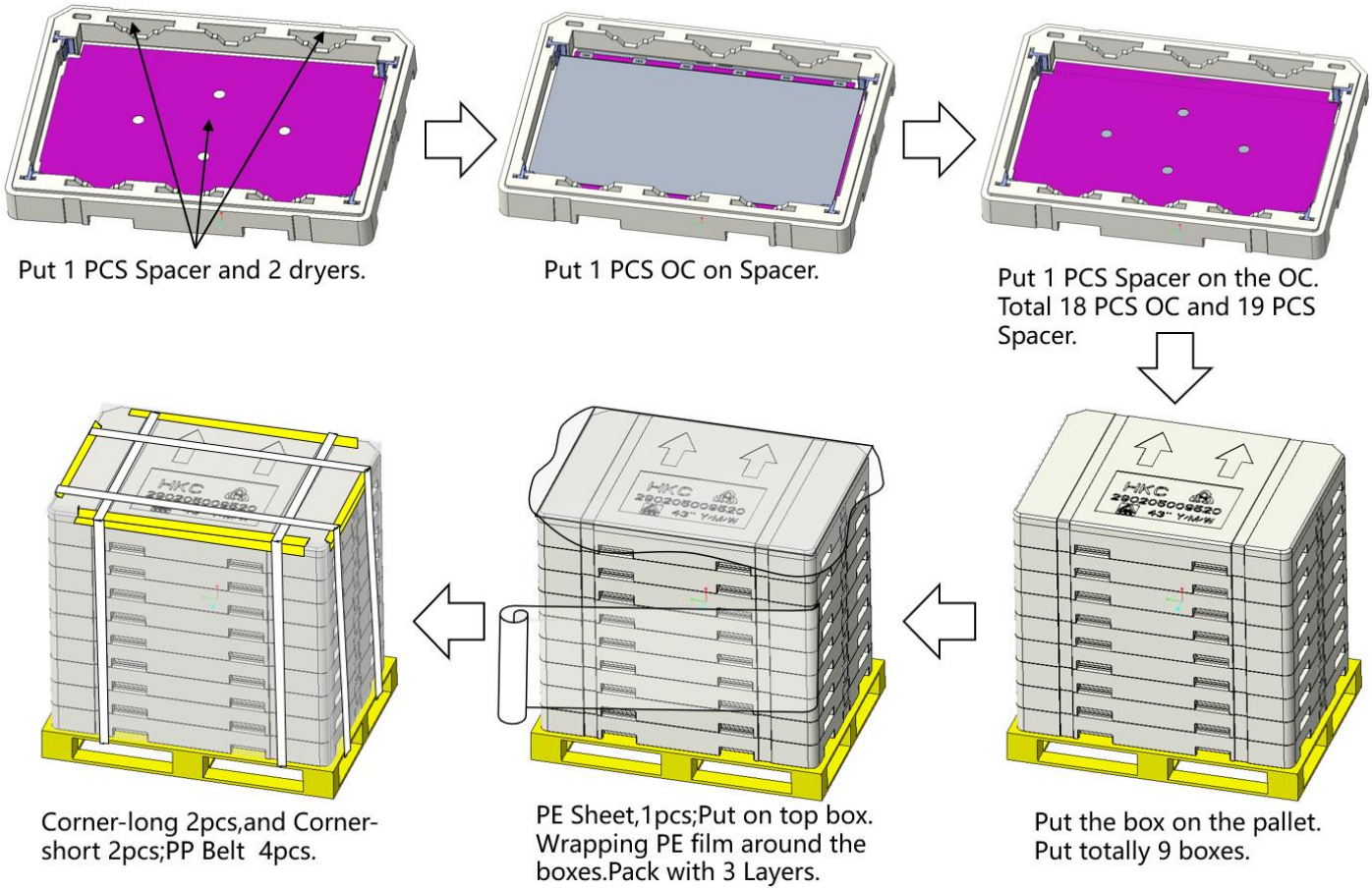
5.2 Packing

5.2.1 Packing Specifications

Item	Specification			
	Quantity		Quantity	
Packing Box	18pcs/box	1100*800*113.5	Net Weight Gross Weight	28.8Kg 32Kg
Pallet	1	1150*850*120	Net Weight	14 Kg
Stack Layer	9			
Boxes per Pallet	9			
Pallet after Packing	162pcs/pallet	1150*850*1092	Gross Weight	303Kg

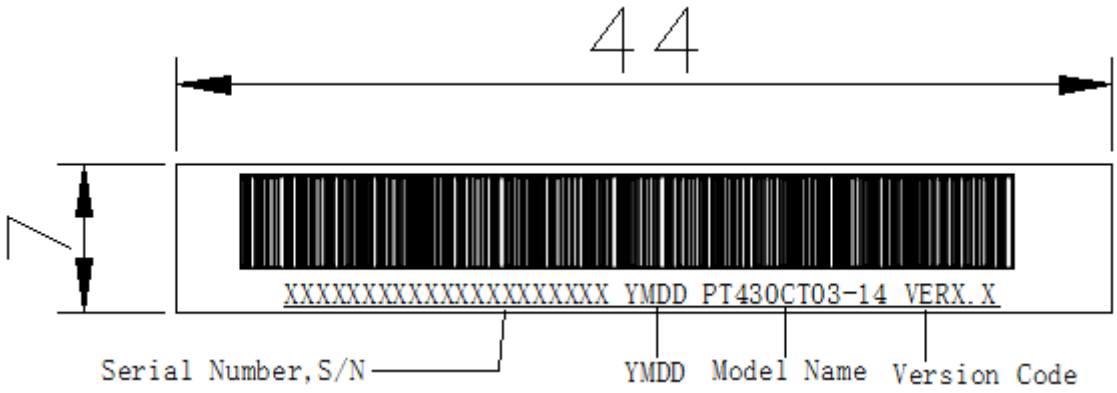
5.2.2 Packing material specification

Item	Specification
Pol protection film peeling force	≦80gf/25mm, 30M/min
Pol protection film material surface resistance	10^6 ~ $10^{9.9}$Ω/□
Box surface resistance	10^6~ $10^{9.9}$ Ω/□
Spacer surface resistance	10^6~ $10^{9.9}$ Ω/□

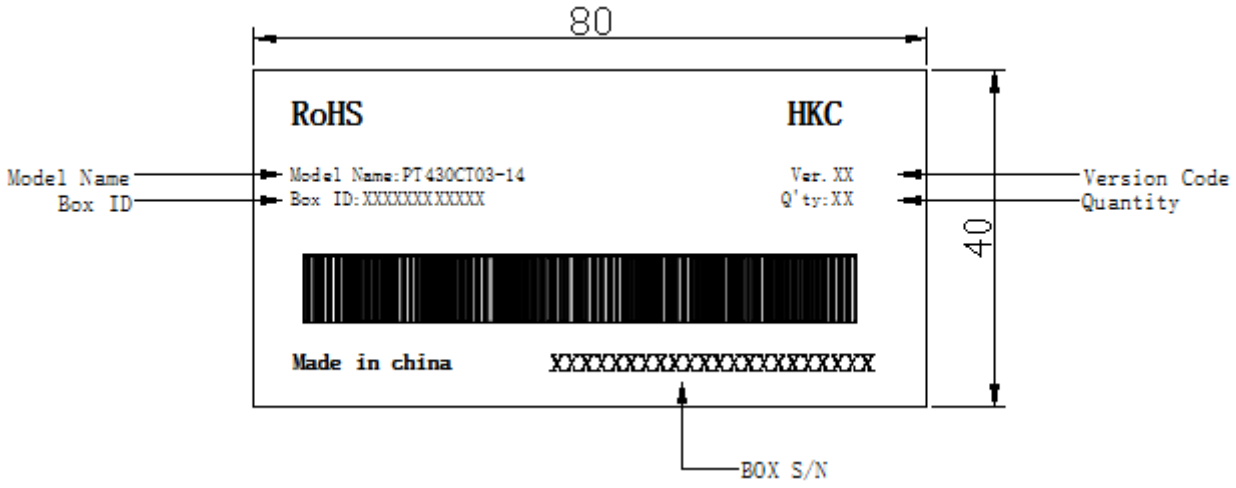


. DEFINITION OF LABELS

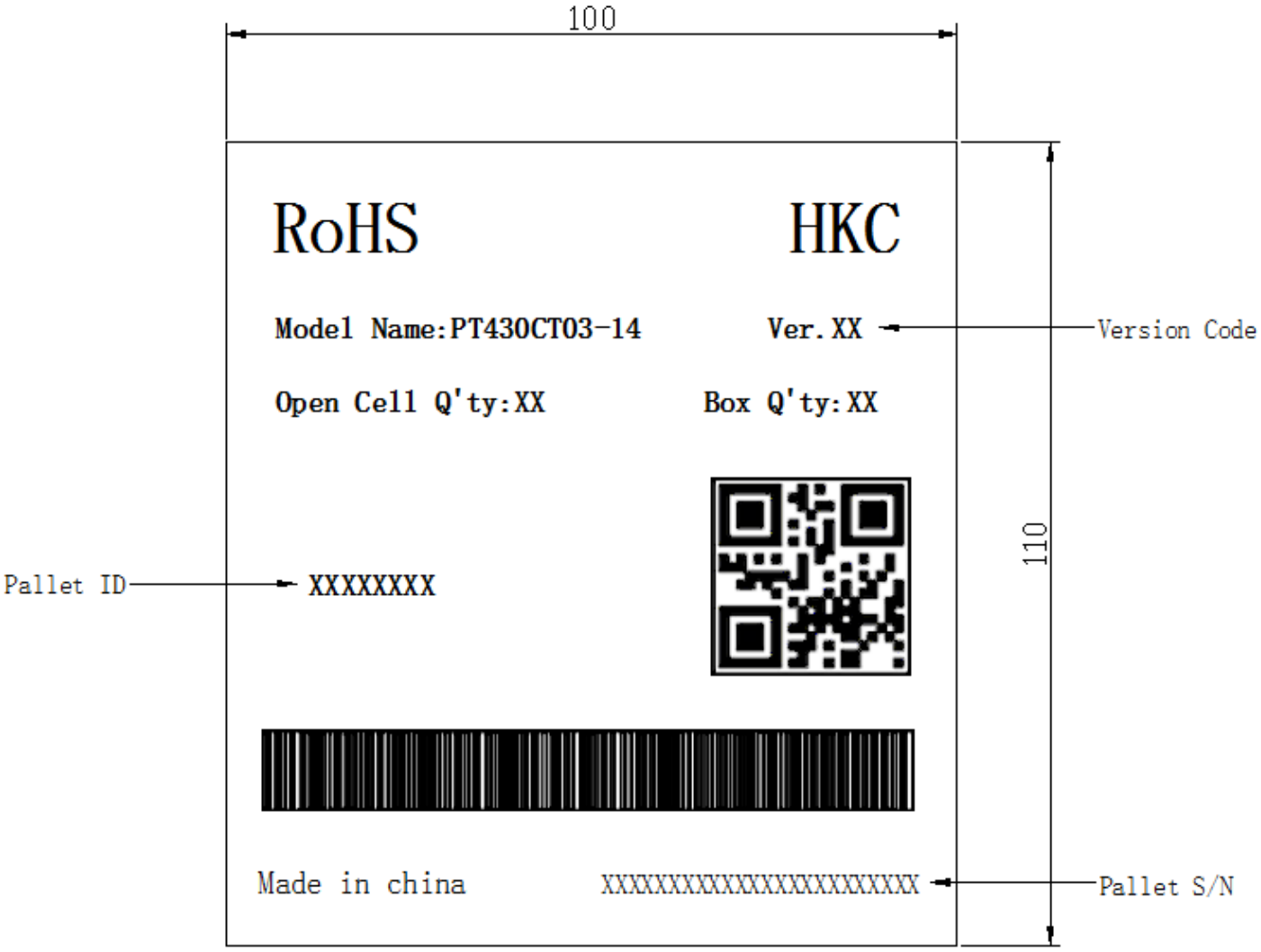
6.1 Open Cell Label



6.2 Carton Label



6.3 Pallet Label



7. PRECAUTION

Please pay attention to the followings when a TFT-LCD cell is used, handled and mounted.

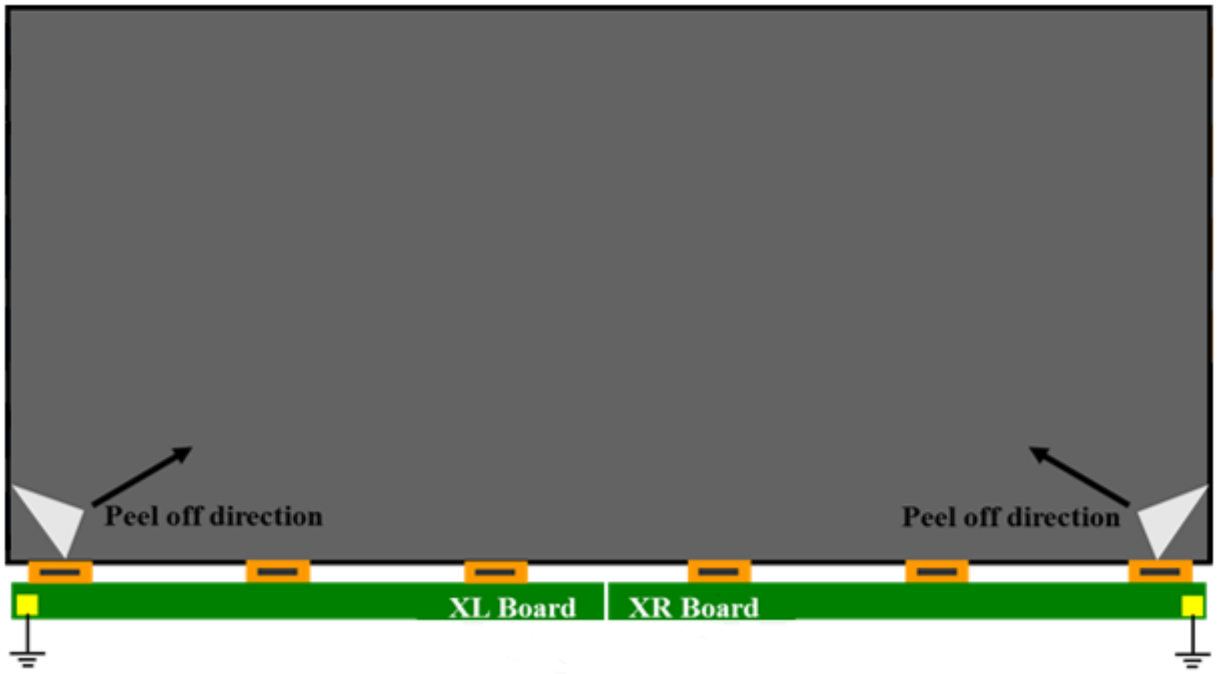
7.1 Unpacking

Should use immediately after unpacking TFT -LCD cell to prevent the terminal corrosion.

Protection film for a polarizer on a TFT open cell should be slowly peeled off so that the electrostatic charge can be minimized.

Source PCB should be connected to the ground when peel off the protection film.

The protection film should not be contacted to the driver during peeling off.



7.2 Storage test

Any attachment on polarizer of open-cell, such as tape, is forbidden and not recommend ,especially under the high temperature and high humidity environment.

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